SSD7317

Advance Information

128 x 96 Dot Matrix OLED/PLED Segment/Common Driver with Integrated Touch Controller

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Appendix: IC Revision history of SSD7317 Specification

Version	Change Items	Effective Date
1.0	1st Release	31-Dec-18
1.1	Update Feature list Update FR formula in section 6.3 Include recommended V_{CC} voltage at LPM in section 7 Update DC Characteristics Table	11-Apr-19
1.2	Updated pin description of DCDCENI and reserved pins Update DC Characteristics Table Update touch description in section 6.10-6.12 Update System Flow	16-Oct-19
1.3	Updated block diagram Updated pin description of ATP[3:0], RX[3:0] and RXT[3:0]. Updated application example	08-Oct-20

CONTENTS

TABLES

FIGURES

1 GENERAL DESCRIPTION

SSD7317 is a single-chip CMOS OLED/PLED driver with Integrated Touch Controller for organic/polymer light emitting diode dot-matrix graphic display system. It consists of 128 segments and 96 commons, and supports In-cell capacitive touch detection on conventional panel structure for 4-key application with plastic or glass cover lens. This IC is designed for Common Cathode type OLED/PLED panel with 4-key touch and 1D slide sensing.

SSD7317 displays data directly from its internal 128 x 96 bits Graphic Display Data RAM (GDDRAM). Data/Commands are sent from general MCU through the hardware selectable I^2C Interface, 6800-/8080-series compatible Parallel Interface or Serial Peripheral Interface. The 256 steps contrast control and oscillator embedded in SSD7317 reduces the number of external components. SSD7317 is designed to support high brightness panel, with maximum source current reaching 600uA, making it suitable for many compact size applications which require high output brightness, such as wearable electronics, smart home device etc.

2 FEATURES

Power Supply

- V_{DD} = 1.65V – 3.5V (for IC logic)
- V_{CI} = 3V – 3.5V (for Touch analog driving, must be greater than or equal to V_{DD})
- V_{CC} = 8V – 18V (for Display panel driving)
- V_{CC} must be higher or equivalent to V_{CI} – 0.6V in Low power mode (LPM).

Display

- Resolution: 128 x 96 dot matrix panel
- Segment maximum source current: 600uA
- Common maximum sink current: 76.8mA
- Embedded 128 x 96 bit SRAM display buffer
- Screen saving continuous scrolling function in both horizontal and vertical direction
- Screen saving infinite content scrolling function
- Internal or external I_{REF} selection
- RAM write synchronization signal
- Programmable Frame Rate and Multiplexing Ratio
- Row Re-mapping and Column Re-mapping
- Power On Reset (POR)
- On-Chip Oscillator
- Dynamic Grayscale

Touch

- Supports In-cell capacitive touch detection on conventional panel structure for 4-key and 1-D slide application
- 16kB firmware-based system operation by host
- Works with all proprietary sensor patterns recommended by SSL for On-cell structure
- Water and moisture immunity:
    - No false touch with condensation or water drop up to 5 mm diameter
    - One-finger tracking with condensation or water drop up to 5 mm diameter
- Large object report flag
- Supports single tap, double taps, long tap, slide gestures
- Supports 4-key touch gloved operation with plastic materials up to 0.2mm thickness

- Scan Speed:
  - Normal mode: typical 105Hz
  - Low power mode (LPM): configurable to allow power and speed optimization
- Programmable timeout for automatic transition from normal to low power mode
- Support out cell application up to 8-key
- Auto calibration

System Interfaces

- Pin selectable for display communication Interfaces:
  - 8 bits 6800/8080-series
  - SPI
  - I^2C
- Pin selectable for touch communication Interfaces:
  - SPI
  - I^2C

Package

- Chip layout for COG
- Wide range of operating temperature: -40°C to 85°C

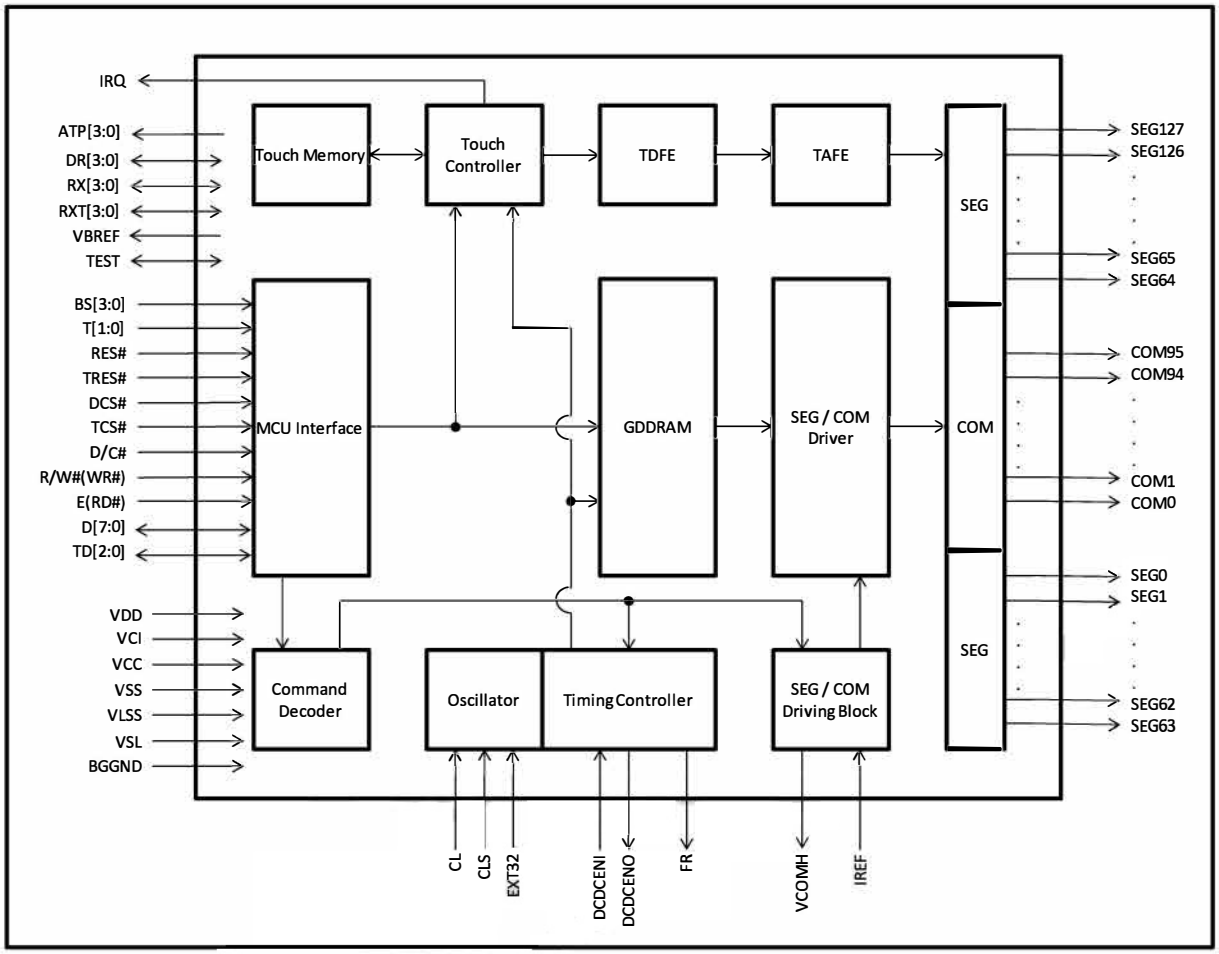
3 ORDERING INFORMATION

Table 3-1: Ordering Information

Ordering Part Number	SEG	COM	Package Form	Remark
SSD7317Z	128	96	COG	o Min SEG pad pitch : 29um o Min COM pad pitch : 35um o Min I/O pad pitch : 55um o Die thickness: 250um o Bump height: nominal 9um

4 BLOCK DIAGRAM

Figure 4-1: SSD7317 Block Diagram



5 PIN DESCRIPTION

Key:

I = Input	NC = Not Connected
O =Output	Pull LOW= connect to Ground
I/O = Bi-directional (input/output)	Pull HIGH= connect to V_{DD}
P = Power pin	

Table 5-1: Pin Description

Pin Name	Pin Type	Description
V_{DD}	P	Power supply pin for core logic operation.
V_{CI}	P	Power supply pin for touch analog driving. V_{CI} must be greater than or equal to V_{DD}.
V_{CC}	P	Power supply for panel driving voltage. This is also the most positive power voltage supply pin.
V_{SS}	P	Ground pin. It must be connected to external ground.
V_{LSS}	P	Analog system ground pin. It must be connected to external ground.
BGGND	P	Reserved pin. It must be connected to ground.
VSL	P	This is segment voltage (output low level) reference pin. When external VSL is not used, this pin must be connected to V_{LSS} externally. When external VSL is used, connect with resistor and diode to ground (depends on application).
V_{LH}	P	Logic high (same voltage level as V_{DD}) for internal connection of input and I/O pins. No need to connect to external power source.
V_{LL}	P	Logic low (same voltage level as V_{SS}) for internal connection of input and I/O pins. No need to connect to external ground.
V_{COMH}	P	COM signal deselected voltage level. A capacitor should be connected between this pin and V_{SS}.
VBREF	O	This is a reserved pin. It should be kept NC.
BS[3:0]	I	MCU bus interface selection pins. Select appropriate logic setting as described in Table 5-2: Bus Interface selection. BS3, BS2, BS1and BS0 are pin select.

Table 5-2: Bus Interface selection

BS[3:0]	Display Interface	Touch Interface
0000	4 line SPI	SPI
0001	3 line SPI	
0010	I^2C	
0100	8-bit 6800 parallel	
0110	8-bit 8080 parallel	
1000	4 line SPI	I^2C
1001	3 line SPI	
1010	I^2C	
1100	8-bit 6800 parallel	
1110	8-bit 8080 parallel	

Note
(1) 0 is connected to V_{SS}
(2) 1 is connected to V_{DD}

Pin Name	Pin Type	Description
I_{REF}	I	This pin is the segment output current reference pin. When I_{REF} is supplied externally, a resistor should be connected between this pin and V_{SS} to maintain the current around 18.75uA. Please refer to Figure 6-16 for the details of resistor value. When internal I_{REF} is used, this pin should be kept NC.
CL	I	This is external clock input pin for display interface. When internal clock is enabled (i.e. HIGH in CLS pin), this pin is not used and should be connected to V_{SS} / V_{LL}. When internal clock is disabled (i.e. LOW in CLS pin), this pin is the external clock source input pin.
CLS	I	This is internal clock enable pin for display interface. When it is pulled HIGH (i.e. connect to V_{DD}), internal clock is enabled. When it is pulled LOW, the internal clock is disabled; an external clock source must be connected to the CL pin for normal operation.
DCS#	I	This pin is the chip select input connecting to the MCU for display interface. The display is enabled for MCU communication only when DCS# is pulled LOW (active LOW).
RES#	I	This pin is the master reset signal input. When the pin is pulled LOW, initialization of the chip is executed. Keep this pin pull HIGH during normal operation.
D/C#	I	This pin is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data at D[7:0] will be interpreted as data. When the pin is pulled LOW, the data at D[7:0] will be transferred to a command register. In I^2C mode, this pin acts as SA0 for slave address selection. When 3-wire serial interface is selected, this pin must be connected to V_{SS} / V_{LL}. For detail relationship to MCU interface signals, refer to Timing Characteristics Diagrams Figure 10-1 to Figure 10-3.
R/W# (WR#)	I	This pin is Read/Write control input pin connecting to the MCU interface. When 6800 interface mode is selected, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I^2C interface is selected, this pin must be connected to V_{SS} / V_{LL}.
E (RD#)	I	This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected. When 8080 interface mode is selected, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected. When serial interface is selected, this pin must be connected to V_{SS} / V_{LL}. In I^2C mode, this pin acts as SA1 for slave address selection.

Pin Name	Pin Type	Description
D[7:0]	I/O	These pins are bi-directional data bus connecting to the MCU data bus for display interface. Unused pins are recommended to tie LOW. When serial interface mode is selected, D2, D1 should be tied together and serves as serial data input: SDIN and D0 is the serial clock input: SCLK; When I^2C mode is selected, D2, D1 should be tied together and serve as SDA_{out}, SDA_{in} in application and D0 is the serial clock input, SCL.
FR	O	This pin outputs RAM write synchronization signal. Proper timing between MCU data writing and frame display timing can be achieved to prevent tearing effect. It should be kept NC if it is not used.
EXT32	I	This is external clock input pin for touch. It should be connected to V_{SS} / V_{LL} if it is not used.
TCS#	I	This pin is the chip select input connecting to the MCU for touch. The touch interface is enabled for MCU communication only when TCS# is pulled LOW (active LOW).
TRES#	I	This pin is the reset signal input for touch. When the pin is pulled LOW, initialization of the touch is executed. Keep this pin pull HIGH during normal operation.
TD[2:0]	I/O	These pins are bi-directional data bus connecting to the MCU data bus for touch interface. Unused pins are recommended to tie LOW. When serial interface mode is selected, TD2 serves as serial data output: SDOUT, TD1 serves as serial data input: SDIN and TD0 is the serial clock input: SCLK; When I C mode is selected, TD2, TD1 should be tied together and serve as SDA_{out}, SDA_{in} in application and TD0 is the serial clock input, SCL.
IRQ	O	Interrupt signal for touch reporting.
TEST	I/O	It should be connected to V_{SS} / V_{LL}.
DCDCENI	I	Enable input pin for external DCDC circuit control. This pin is recommended to tie V_{DD}. When it is pulled HIGH (i.e. connect to V_{DD}), DCDCENO pin can be controlled by firmware or command.
DCDCENO	O	Enable output pin for external DCDC circuit. It should be kept NC if it is not used.
T0, T1	I/O	Reserved pin. It should be kept NC.
SEG0 ~ SEG127	O	These pins provide the OLED segment driving signals. These pins are V_{SS} state when display is OFF.
COM0 ~ COM95	O	These pins provide the Common switch signals to the OLED panel. These pins are in high impedance state when display is OFF.
DR[3:0]	-	Reserved pins, it should be kept NC if it is not used.

Pin Name	Pin Type	Description
ATP[3:0]	-	It must be connected to external FPC to GND separately OR reserve test pad on FPC.
RX[3:0]	-	Outcell touch sensing channel.
RXT[3:0]	-	Oncell touch sensing channel.
SHA ~ SHN	-	Reserved pins, it should be kept NC.
V33	P	Same voltage level as VCC. No need to connect to external power source.
V38	P	Same voltage level as VCOMH. No need to connect to external power source.
TR[19:0]	-	Reserved pin. It should be kept NC.
NC	-	This is dummy pin. It should be kept NC.

6 FUNCTIONAL BLOCK DESCRIPTIONS

6.1 Display Interface Selection

SSD7317 display interface consist of 8 data pins and 5 control pins. The pin assignment at different interface mode is summarized in Table 6-1. Different display interface mode can be set by hardware selection on BS[3:0] pins.

Table 6-1: Display interface assignment under different bus interface mode

Pin Name / Bus Interface	Data/Command Interface								Control Signal				
	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W#	DCS#	D/C#	RES#
8-bit 8080	D[7:0]								RD#	WR#	DCS#	D/C#	RES#
8-bit 6800	D[7:0]								E	R/W#	DCS#	D/C#	RES#
3-wire SPI	Tie LOW					SDIN		SCLK	Tie LOW		DCS#	Tie LOW	RES#
4-wire SPI	Tie LOW					SDIN		SCLK	Tie LOW		DCS#	D/C#	RES#
I^2C	Tie LOW					SDA_{OUT}	SDA_{IN}	SCL	SA1	Tie LOW		SA0	RES#

6.1.1 Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), R/W#, D/C#, E and DCS#.

A LOW in R/W# indicates WRITE operation and HIGH in R/W# indicates READ operation.
A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
The E input serves as data latch signal while DCS# is LOW. Data is latched at the falling edge of E signal.

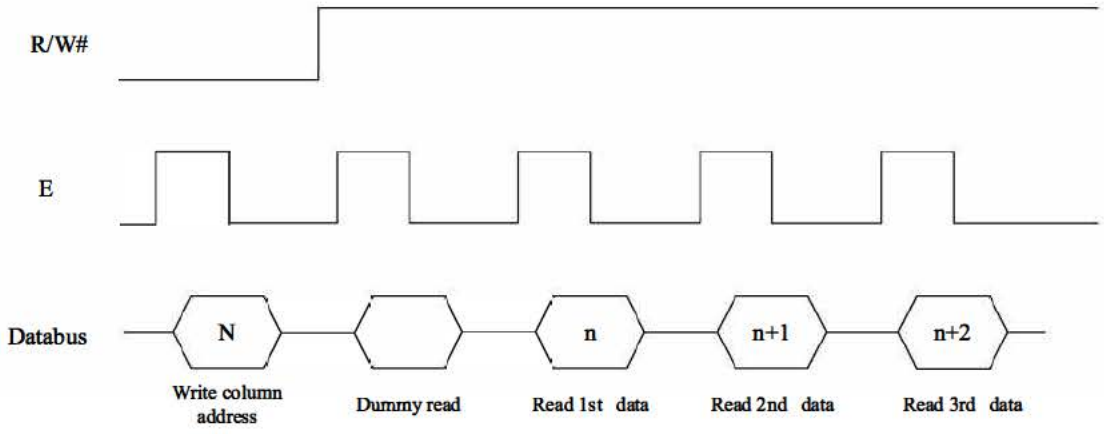
Table 6-2: Control pins of 6800 interface

Function	E	R/W#	DCS#	D/C#
Write command	↓	L	L	L
Read status	↓	H	L	L
Write data	↓	L	L	H
Read data	↓	H	L	H

Note
(1) ↓ stands for falling edge of signal
H stands for HIGH in signal
L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 6-1.

Figure 6-1: Data read back procedure - insertion of dummy read



6.1.2 Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), RD#, WR#, D/C# and DCS#.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
A rising edge of RD# input serves as a data READ latch signal while DCS# is kept LOW.
A rising edge of WR# input serves as a data/command WRITE latch signal while DCS# is kept LOW.

Figure 6-2: Example of Write procedure in 8080 parallel interface mode

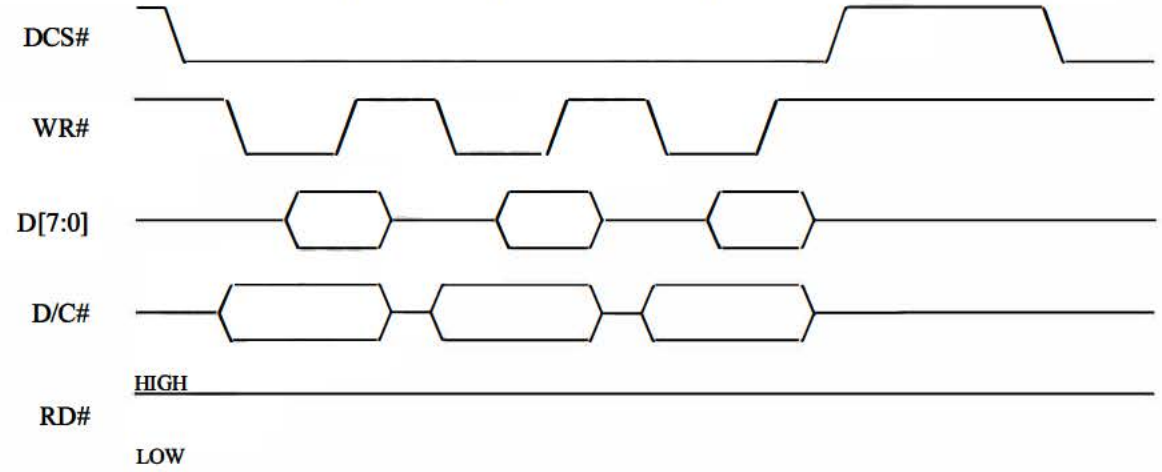


Figure 6-3: Example of Read procedure in 8080 parallel interface mode

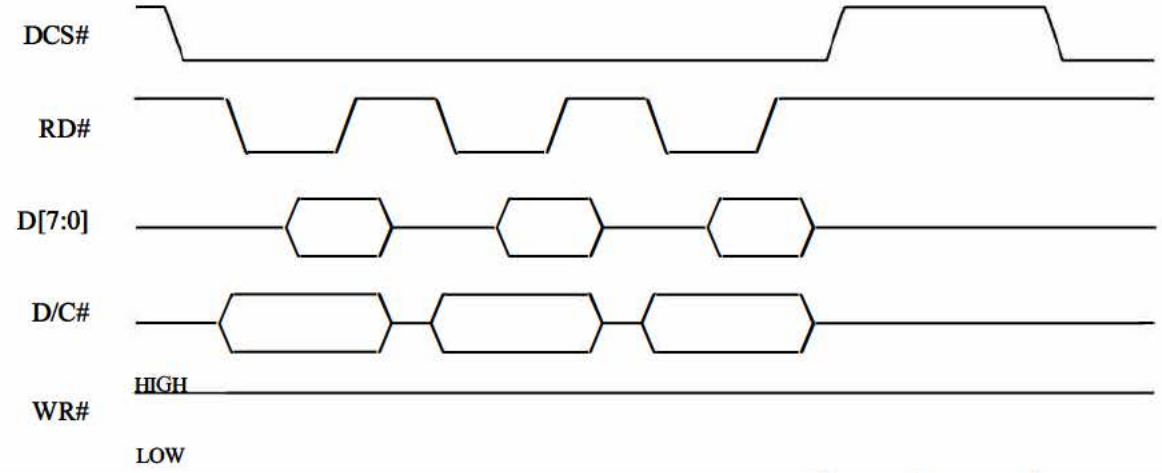


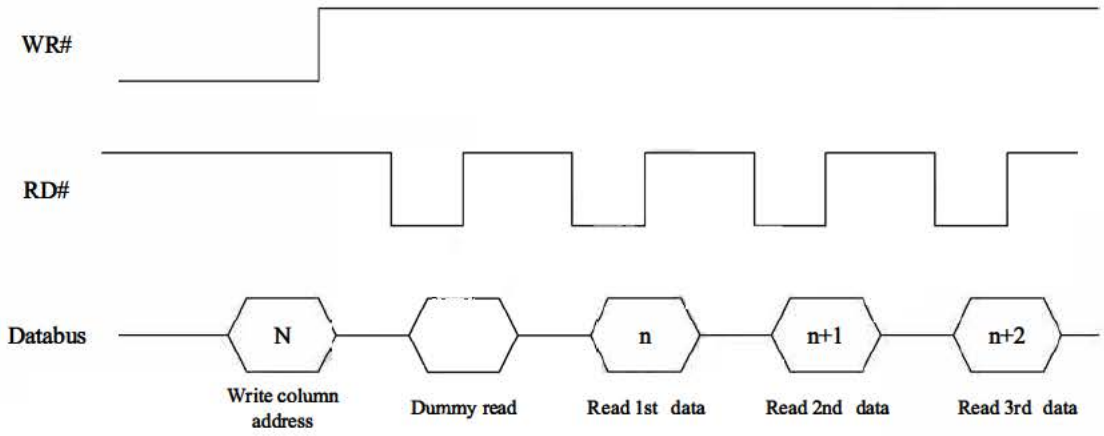
Table 6-3: Control pins of 8080 interface

Function	RD#	WR#	DCS#	D/C#
Write command	H	↑	L	L
Read status	↑	H	L	L
Write data	H	↑	L	H
Read data	↑	H	L	H

Note
(1) ↑ stands for rising edge of signal
(2) H stands for HIGH in signal
(3) L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 6-4.

Figure 6-4: Display data read back procedure - insertion of dummy read



6.1.3 Serial Interface (4-wire SPI)

The 4-wire serial interface consists of serial clock: SCLK, serial data: SDIN, D/C#, DCS#. In 4-wire SPI mode, D0 acts as SCLK, D1, D2 are tied together to act as SDIN. For the unused data pins from D3 to D7, E(RD#) and R/W#(WR#) can be connected to an external ground.

Table 6-4: Control pins of 4-wire Serial interface

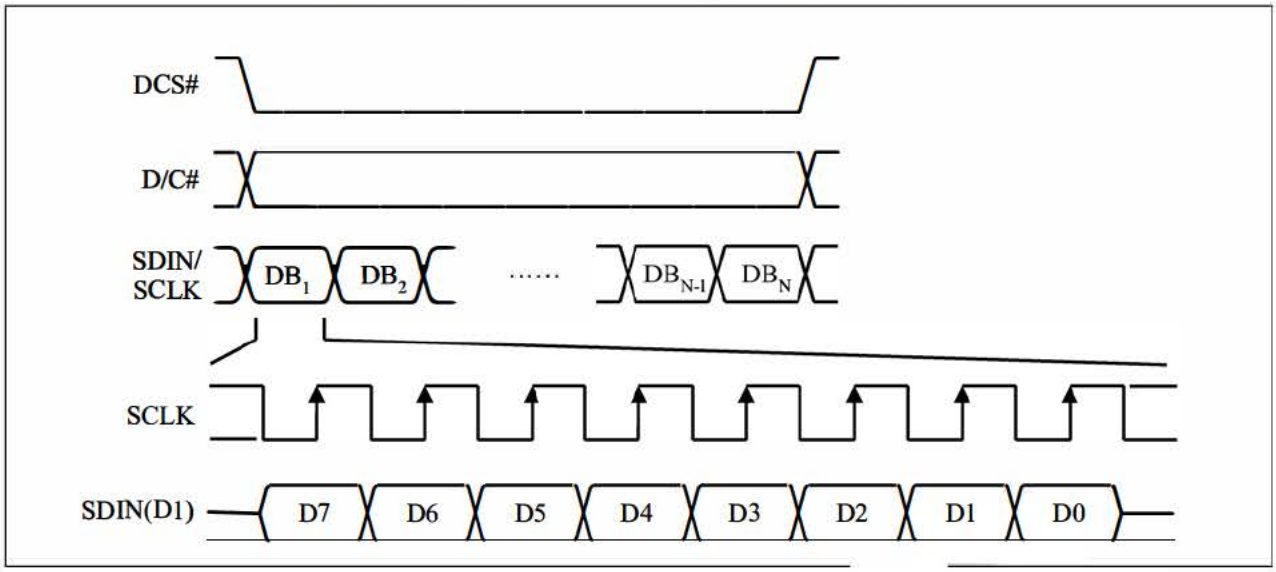
Function	E	R/W#	DCS#	D/C#	D0
Write command	Tie LOW	Tie LOW	L	L	↑
Write data	Tie LOW	Tie LOW	L	H	↑

Note
(1) H stands for HIGH in signal
(2) L stands for LOW in signal
(3) ↑ stands for rising edge of signal

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... , D0. D/C# is sampled on every eighth clock and D/C# should be kept stable throughout eight clock period. The data byte in the shift register is written to the Graphic Display Data RAM (GDDRAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

Figure 6-5: Write procedure in 4-wire Serial interface mode



6.1.4 Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and DCS#.
In 3-wire SPI mode, D0 acts as SCLK, D1, D2 are tied together to act as SDIN. For the unused data pins from D3 to D7, R/W# (WR#), E(RD#) and D/C# can be connected to an external ground.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit 1) or the command register (D/C# bit 0).

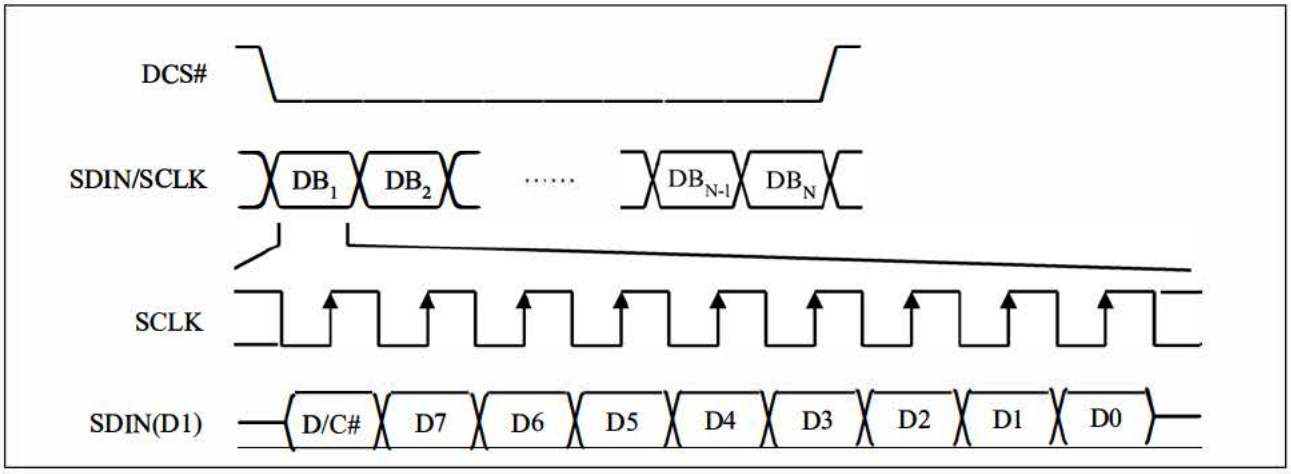
Under serial mode, only write operations are allowed.

Table 6-5: Control pins of 3-wire Serial interface

Function	E(RD#)	R/W#(WR#)	DCS#	D/C#	D0
Write command	Tie LOW	Tie LOW	L	Tie LOW	↑
Write data	Tie LOW	Tie LOW	L	Tie LOW	↑

Note
(1) L stands for LOW in signal
(2) ↑ stands for rising edge of signal

Figure 6-6: Write procedure in 3-wire Serial interface mode



6.1.5 I²C Interface

The I²C communication interface consists of slave address bits SA[1:0], I²C-bus data signal SDA (SDA_{OUT}/D_2 for output and SDA_{IN}/D_1 for input) and I²C-bus clock signal SCL (D_0). Both the data and clock signals must be connected to pull-up resistors. RES# is used for the initialization of device.

a) Slave address bits (SA[1:0])
SSD7317 has to recognize the slave address before transmitting or receiving any information by the I²C-bus. The device will respond to the slave address following by the slave address bits (SA[1:0]) and the read/write select bit ("R/W#" bit) with the following byte format:

b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
0	1	1	1	1	SA1	SA0	R/W#

SA[1:0] bits provide extension bits for the slave address. "b0111100" or "b0111101" or "b0111110" or "b0111111", can be selected as the slave address of SSD7317. E pin acts as SA1 and D/C# pin acts as SA0 for slave address selection.
"R/W#" bit is used to determine the operation mode of the I²C-bus interface. R/W# = 1, it is in read mode. R/W# = 0, it is in write mode.

b) I²C-bus data signal (SDA)
SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA.

It should be noticed that the ITO track resistance and the pulled-up resistance at "SDA" pin becomes a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in "SDA".

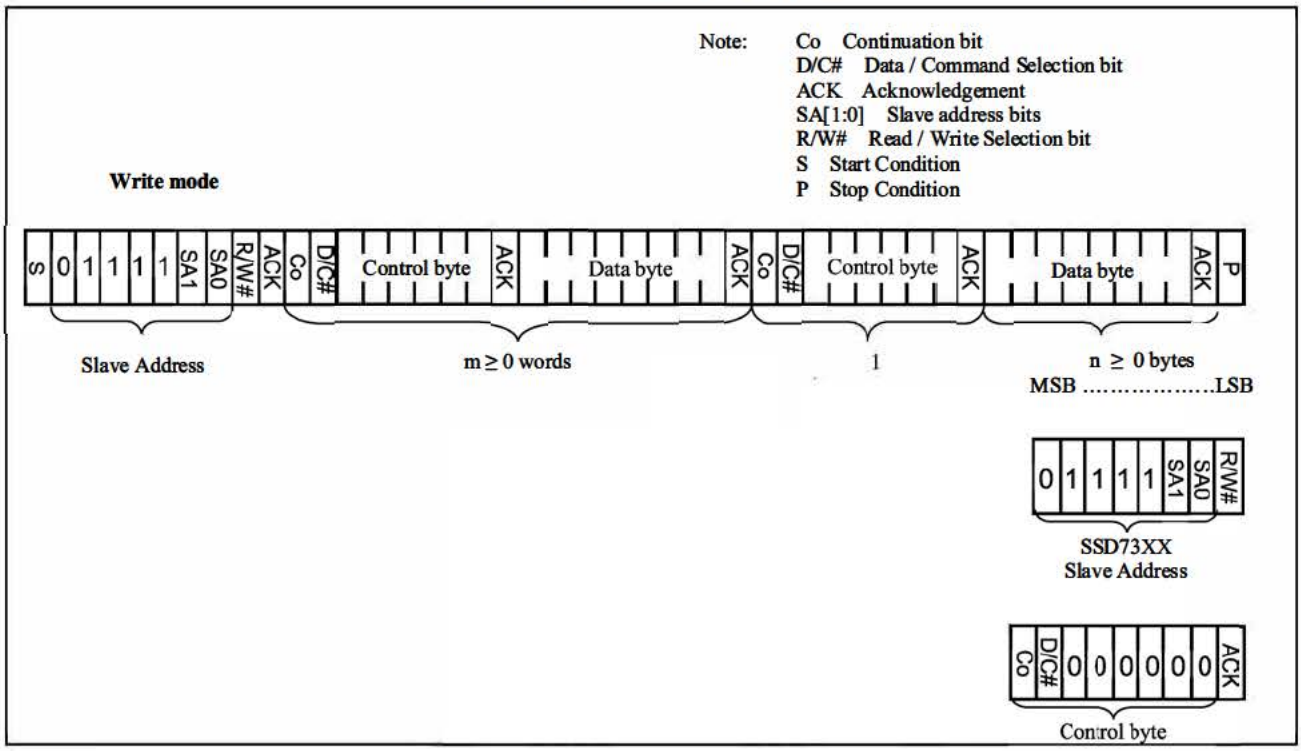
"SDA_{IN}" and "SDA_{OUT}" are tied together and serve as SDA. The "SDA_{IN}" pin must be connected to act as SDA. The "SDA_{OUT}" pin may be disconnected. When "SDA_{OUT}" pin is disconnected, the acknowledgement signal will be ignored in the I²C-bus.

c) I²C-bus clock signal (SCL)
The transmission of information in the I²C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

6.1.5.1 I²C-bus Write Data

The I²C-bus interface gives access to write data and command into the device. Please refer to for the write mode of I²C-bus in chronological order.

Figure 6-7: I²C-bus data format



6.1.5.2 Write mode for I²C

1) The master device initiates the data communication by a start condition. The definition of the start condition is shown in Figure 6-8. The start condition is established by pulling the SDA from HIGH to LOW while the SCL stays HIGH.
2) The slave address is following the start condition for recognition use. For the SSD7317, the slave address is "b0111100" or "b0111101" or "b0111110" or "b0111111" by changing the SA[1:0] to LOW or HIGH (E pin acts as SA1 and D/C pin acts as SA0).
3) The write mode is established by setting the R/W# bit to logic "0".
4) An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. Please refer to the Figure 6-9 for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.
5) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six "0" 's.
    a. If the Co bit is set as logic "0", the transmission of the following information will contain data bytes only.
    b. The D/C# bit determines the next data byte is acted as a command or a data. If the D/C# bit is set to logic "0", it defines the following data byte as a command. If the D/C# bit is set to logic "1", it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.
6) Acknowledge bit will be generated after receiving each control byte or data byte.
7) The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 6-8. The stop condition is established by pulling the "SDA in" from LOW to HIGH while the "SCL" stays HIGH.

Figure 6-8: Definition of the Start and Stop Condition

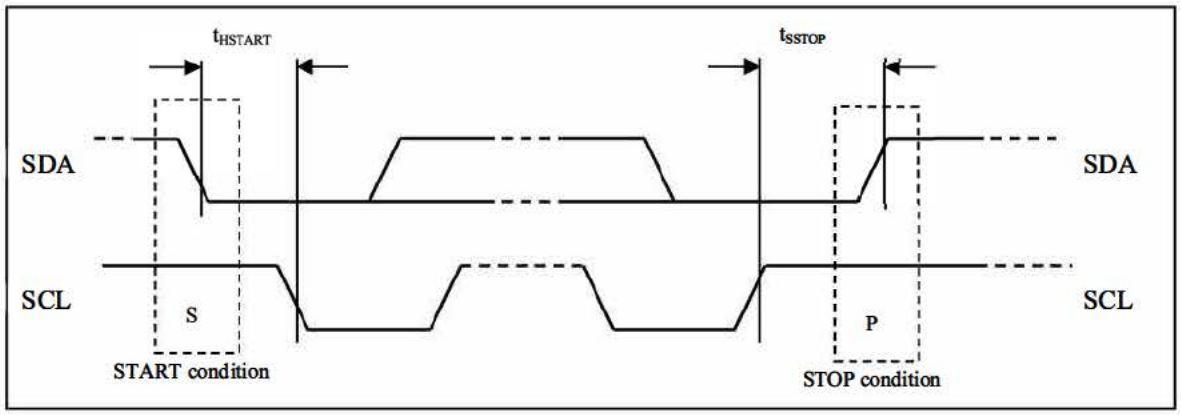
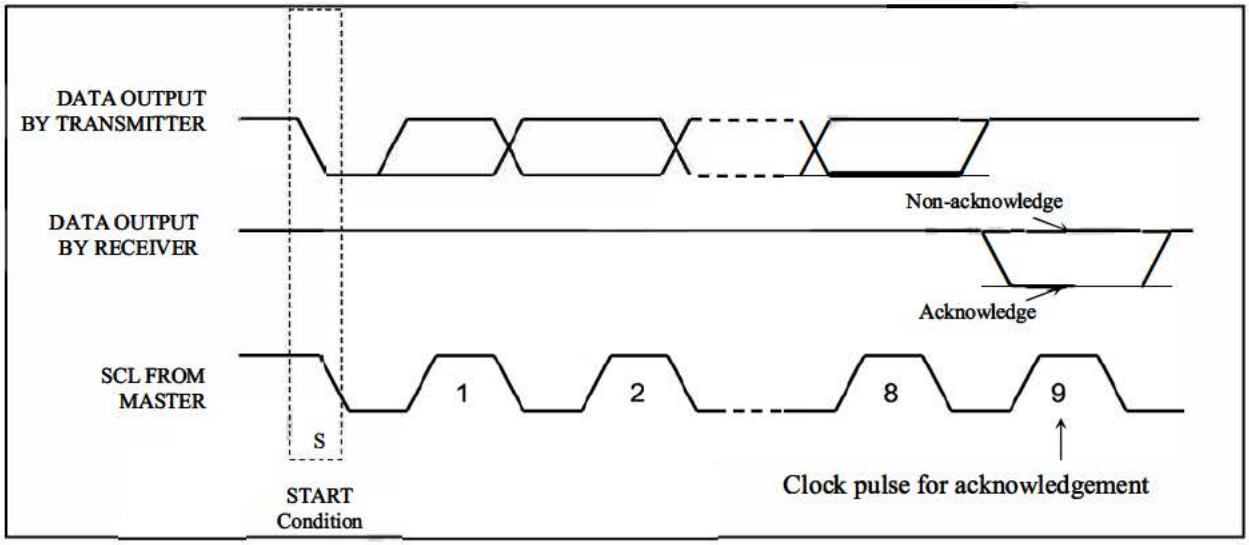


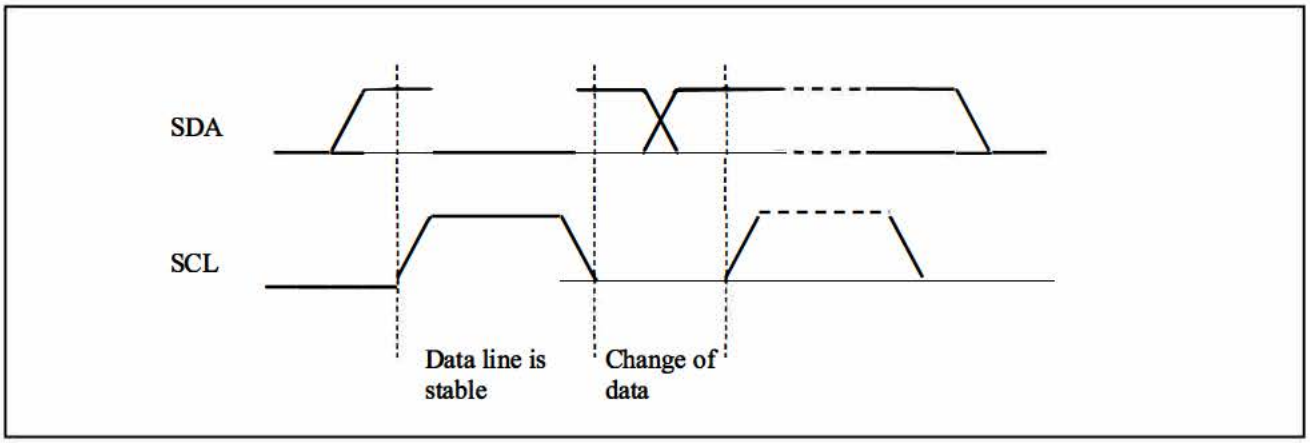
Figure 6-9: Definition of the acknowledgement condition



Please be noted that the transmission of the data bit has some limitations.

1. The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the "HIGH" period of the clock pulse. Please refer to the Figure 6-10 for graphical representations. Except in start or stop conditions, the data line can be switched only when the SCL is LOW.
2. Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.

Figure 6-10: Definition of the data transfer condition



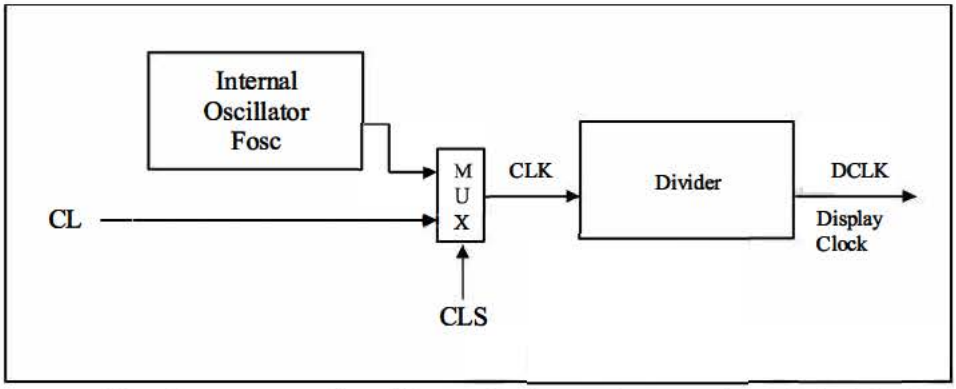
6.2 Command Decoder

This module determines whether the input data is interpreted as data or command. Data is interpreted based upon the input of the D/C# pin.

If D/C# pin is HIGH, D[7:0] is interpreted as display data written to Graphic Display Data RAM (GDDRAM). If it is LOW, the input at D[7:0] is interpreted as a command. Then data input will be decoded and written to the corresponding command register.

6.3 Oscillator Circuit and Display Time Generator

Figure 6-11: Oscillator Circuit and Display Time Generator



This module is an on-chip LOW power RC oscillator circuitry. The operation clock (CLK) can be generated either from internal oscillator or external source CL pin. This selection is done by CLS pin. If CLS pin is pulled HIGH, internal oscillator is chosen and CL should be connected to V_{SS}. Pulling CLS pin LOW disables internal oscillator and external clock must be connected to CL pins for proper operation. When the internal oscillator is selected, its output frequency F_{OSC} can be changed by commands D5h A[7:4],

The display clock (DCLK) for the Display Timing Generator is derived from CLK. The division factor "D" can be programmed from 1 to 16 by command D5h. When D5h A[7:4] is in default setting,

$$DCLK \quad F_{OSC} / 7 / D$$

The frame frequency of display is determined by the following formula:

$$F_{FRM} \quad 1 / [(K \times No.\ of\ Mux / DCLK) + dt]$$

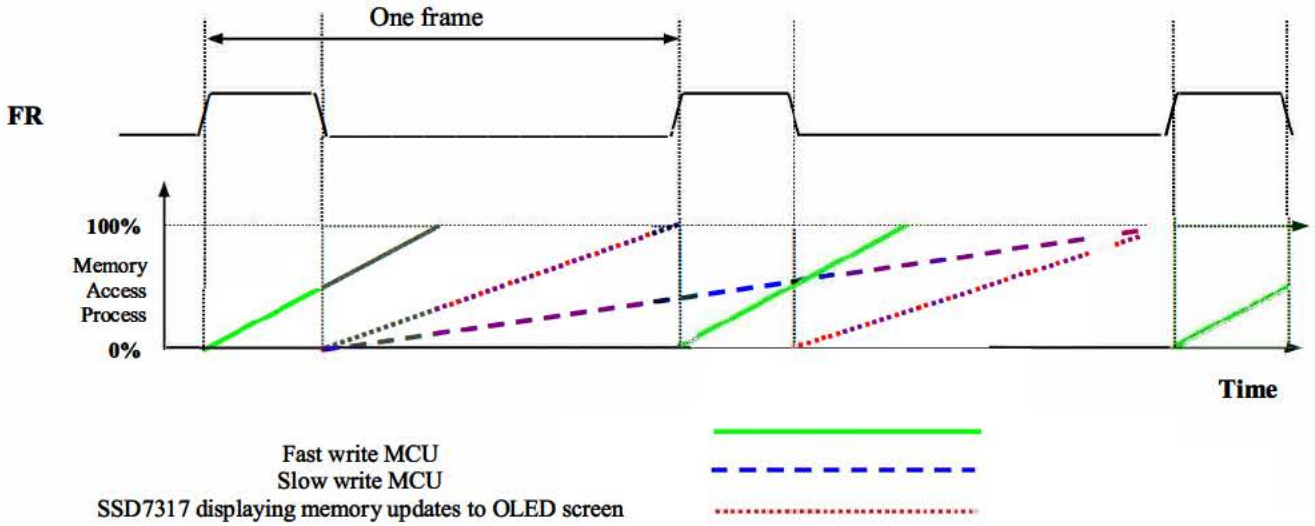
where

- F_{OSC} is the oscillator frequency. It can be changed by command D5h A[7:4].
- D stands for clock divide ratio. It is set by command D5h A[3:0]. The divide ratio has the range from 1 to 16.
- K is the number of display clocks per row. The value is derived by
  K Phase 1 period + Phase 2 period + K_0 4 + 4 + 93 101 at power on reset (i.e. K_0 93). Please refer to Section 6.6 for the details of the "Phase".
- Number of multiplex ratio is set by command A8h. The power on reset value is 95 (i.e. 96MUX).
- dt is the touch time period.

6.4 FR Synchronization

FR synchronization signal can be used to prevent tearing effect.

Figure 6-12: FR Synchronization



The starting time to write a new image to OLED driver is depended on the MCU writing speed. If MCU can finish writing a frame image within one frame period, it is classified as fast write MCU. For MCU needs longer writing time to complete (more than one frame but within two frames), it is a slow write one.

For fast write MCU: MCU should start to write new frame of ram data just after rising edge of FR pulse and should be finished well before the rising edge of the next FR pulse.

For slow write MCU: MCU should start to write new frame ram data after the falling edge of the 1st FR pulse and must be finished before the rising edge of the 3rd FR pulse.

6.5 Reset Circuit

When RES# input is LOW, the chip will be initialized with the following status:

1. Display is OFF
2. 128 x 96 Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00h and COM0 mapped to address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

Touch initialization and firmware should be send again after reset.

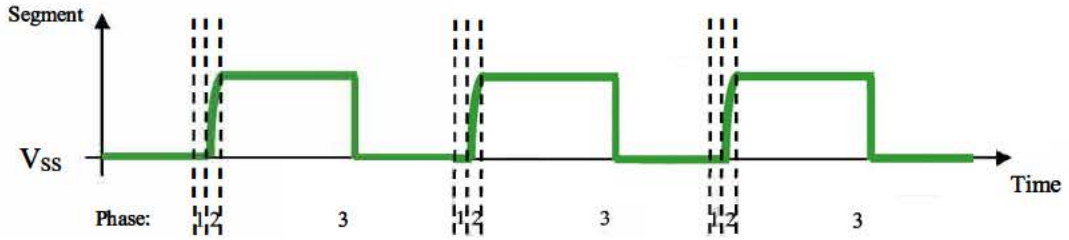
6.6 Segment Drivers / Common Drivers

Segment drivers deliver 128 current sources to drive the OLED panel. The driving current can be adjusted by altering the registers of the contrast setting command (81h). Common drivers generate voltage-scanning pulses.

The segment driving waveform is divided into three phases:

1. In phase 1, the OLED pixel charges of previous image are discharged in order to prepare for next image content display.
2. In phase 2, the OLED pixel is driven to the targeted voltage. The pixel is driven to attain the corresponding voltage level from V_{SS}. The period of phase 2 can be programmed in length from 2 to 30 DCLKs. If the capacitance value of the pixel of OLED panel is larger, a longer period is required to charge up the capacitor to reach the desired voltage.
3. In phase 3, the OLED driver switches to use current source to drive the OLED pixels and this is the current drive stage.

Figure 6-13: Segment Output Waveform in three phases



After finishing phase 3, the driver IC will go back to phase 1 to display the next row image data. This three-step cycle is run continuously to refresh image display on OLED panel.

In phase 3, if the length of current drive pulse width is set to 93, after finishing 93 DCLKs in current drive phase, the driver IC will go back to phase 1 for next row display.

6.7 Graphic Display Data RAM (GDDRAM)

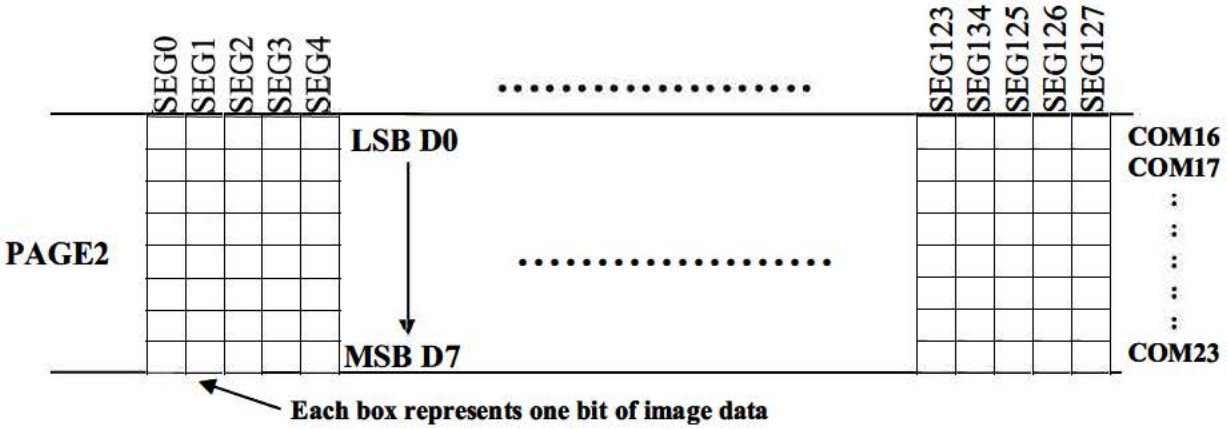
The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128 x 96 bits and the RAM is divided into eight pages, from PAGE0 to PAGE11, which are used for monochrome 128x96 dot matrix display, as shown in Figure 6-14.

Figure 6-14: GDDRAM pages structure

		Row re-mapping
PAGE0 (COM0-COM7)	Page 0	PAGE0 (COM95-COM88)
PAGE1 (COM8-COM15)	Page 1	PAGE1 (COM87-COM80)
PAGE2 (COM16-COM23)	Page 2	PAGE2 (COM79-COM72)
PAGE3 (COM24-COM31)	Page 3	PAGE3 (COM71-COM64)
PAGE4 (COM32-COM39)	Page 4	PAGE4 (COM63-COM56)
PAGE5 (COM40-COM47)	Page 5	PAGE5 (COM55-COM48)
PAGE6 (COM48–COM55)	Page 6	PAGE6 (COM47-COM40)
PAGE7 (COM56-COM63)	Page 7	PAGE7 (COM39-COM32)
PAGE8 (COM64-COM71)	Page 8	PAGE8 (COM31-COM24)
PAGE9 (COM72-COM79)	Page 9	PAGE9 (COM23-COM16)
PAGE10 (COM80–COM87)	Page 10	PAGE10 (COM15-COM8)
PAGE11 (COM88-COM95)	Page 11	PAGE11 (COM 7-COM0)
	SEG0 ----------SEG127	
Column re-mapping	SEG127 ----------SEG0	

When one data byte is written into GDDRAM, all the rows image data of the same page of the current column are filled (i.e. the whole column (8 bits) pointed by the column address pointer is filled.). Data bit D0 is written into the top row, while data bit D7 is written into bottom row as shown in Figure 6-15.

Figure 6-15: Enlargement of GDDRAM (No row re-mapping and column-remapping)



For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software as shown in Figure 6-14.

For vertical shifting of the display, an internal register storing the display start line can be set to control the portion of the RAM data to be mapped to the display (command D3h).

6.8 SEG/COM Driving block

This block is used to derive the incoming power sources into the different levels of internal use voltage and current.

- V_{CC} is the most positive voltage supply.
- V_{COMH} is the Common deselected level. It is internally regulated.
- V_{LSS} is the ground path of the analog and panel current.
- I_{REF} is a reference current source for segment current drivers I_{SEG}. The relationship between reference current and segment current of a color is:

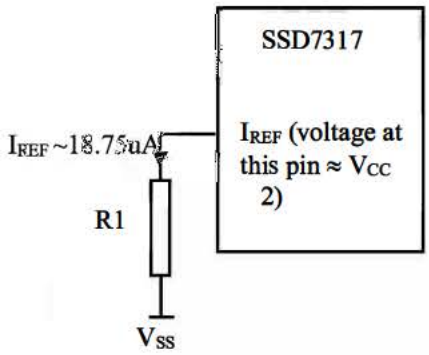
  I_{SEG} = Contrast / 8 x I_{REF}

  in which the contrast (1~255) is set by Set Contrast command 81h

  When internal I_{REF} is used, the I_{REF} pin should be kept NC.
  Bit A[4] of command ADh is used to select external or internal I_{REF} :
  A[4] = '0' Select external I_{REF} [Reset]
  A[4] = '1' Enable internal I_{REF} during display ON

When external I_{REF} is used, the magnitude of I_{REF} is controlled by the value of resistor, which is connected between I_{REF} pin and V_{SS} as shown in Figure 6-16. It is recommended to set I_{REF} to 18.75 ± 2uA so as to achieve I_{SEG} = 600uA at maximum contrast 255.

Figure 6-16: I_{REF} Current Setting by Resistor Value



Since the voltage at I_{REF} pin is V_{CC} – 2V, the value of resistor R1 can be found as below:

For I_{REF} = 18.75uA, V_{CC} =12V:

R1 = (Voltage at I_{REF} – V_{SS}) / I_{REF}
≈ (12 – 2) / 18.75uA
= 530kΩ

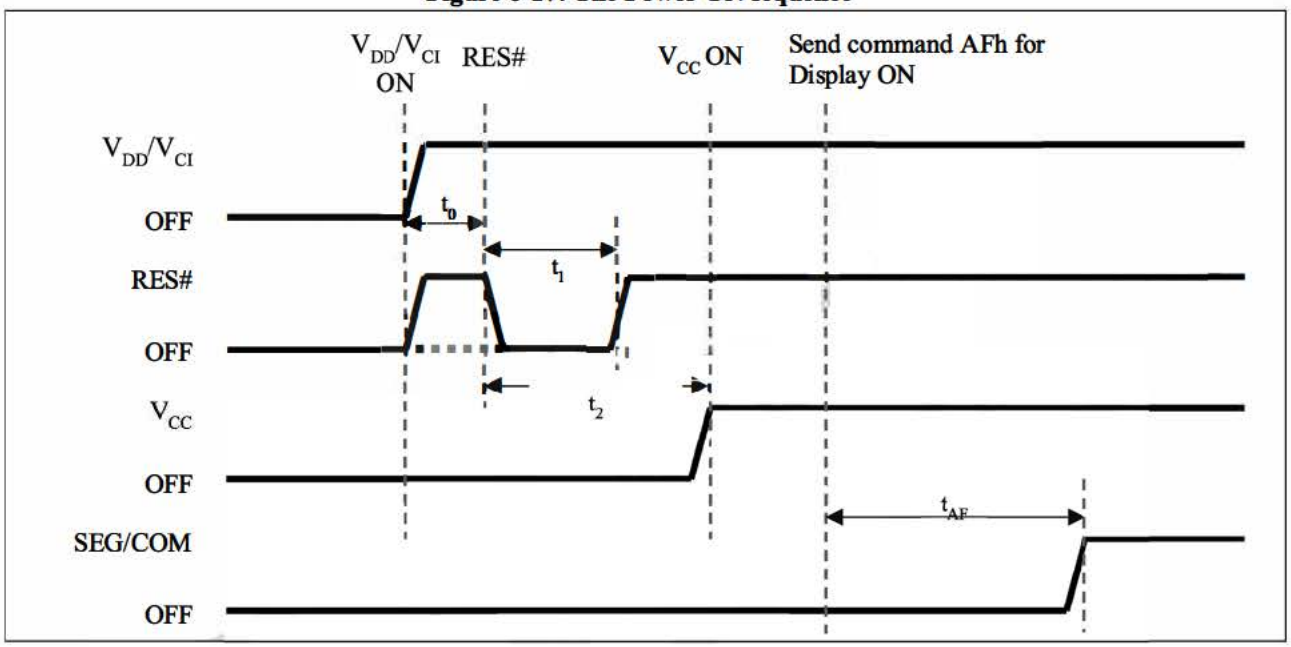
6.9 Power ON and OFF sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD7317.

Power ON sequence:

1. Power ON V_{DD} and V_{CI}. (V_{CI} must be greater than or equal to V_{DD})
2. After V_{DD} and V_{CI} become stable, wait at least 20ms (t_0), set RES# pin LOW (logic low) for at least 3us (t_1) [4] and then HIGH (logic high).
3. After setting RES# pin LOW (logic low), wait for at least 3us (t_2). Then Power ON V_{CC}.[1]
4. After V_{CC} becomes stable, send command AFh for display ON. SEG/COM will be ON after 40ms (t_{AF}).

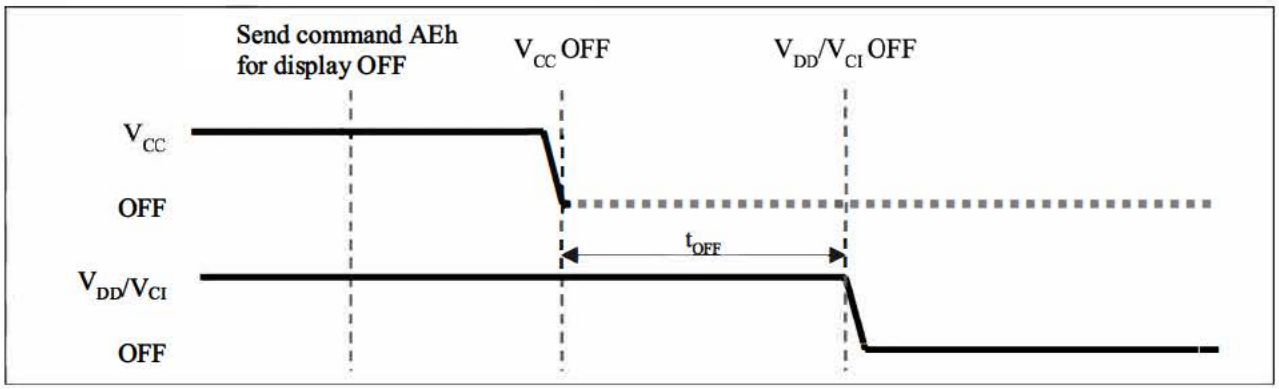
Figure 6-17: The Power ON sequence



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC}.[1], [2]
3. Power OFF V_{DD} and V_{CI} after t_{OFF}. [4] (where Minimum t_{OFF}=0ms, typical t_{OFF}=100ms)

Figure 6-18: The Power OFF sequence



Note:

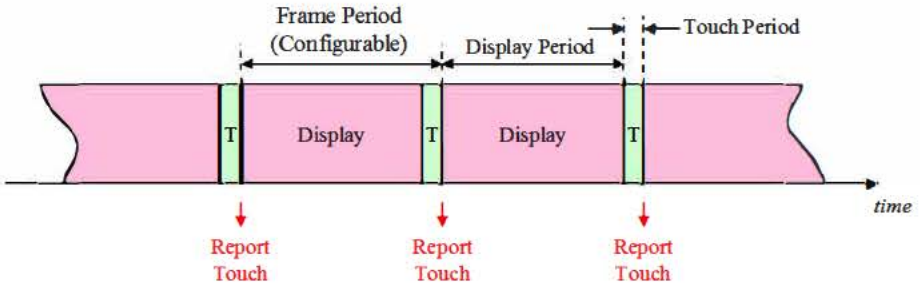
[1] V_{CC} should be kept float (i.e. disable) when it is OFF.
[2] Power Pins (V_{DD}, V_{CI}, V_{CC}) can never be pulled to ground under any circumstance.
[3] The register values are reset after t_1.
[4] V_{DD}, V_{CI} should not be Power OFF before V_{CC} Power OFF.

6.10 Touch Analog Front-end (TAFE)

Touch Analog Front-end is used to detect touch on the panel.

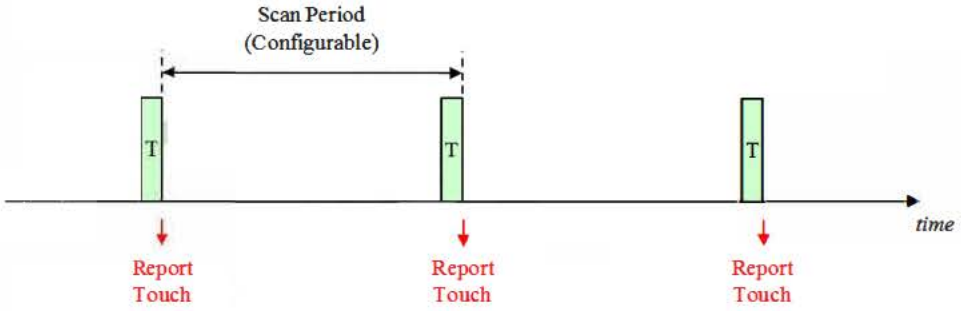
When display is on (Normal Mode), segment driving are multiplexed in time slots for display and touch sensing. Touch gesture is reported at the end of every touch time slot.

Figure 6-19: Frame Scan during display ON (Normal Mode)



When display is off (Low Power Mode), only touch sensing takes place at a lower scan rate (which is configurable to allow power and speed optimization). Touch gesture is reported at the end of every touch time slot.

Figure 6-20: Frame Scan during display OFF (Low Power Mode)



6.11 Touch Digital Front-end (TDFE)

Digital data of the sensing signal from ADC is processed to generate touch data and gesture report. If touch data is greater than the minimum finger level, "1" will be flagged in "Gesture report". The touch data and gesture report are then passed to Command Decoder for read back through the touch interface.

6.12 Touch Memory

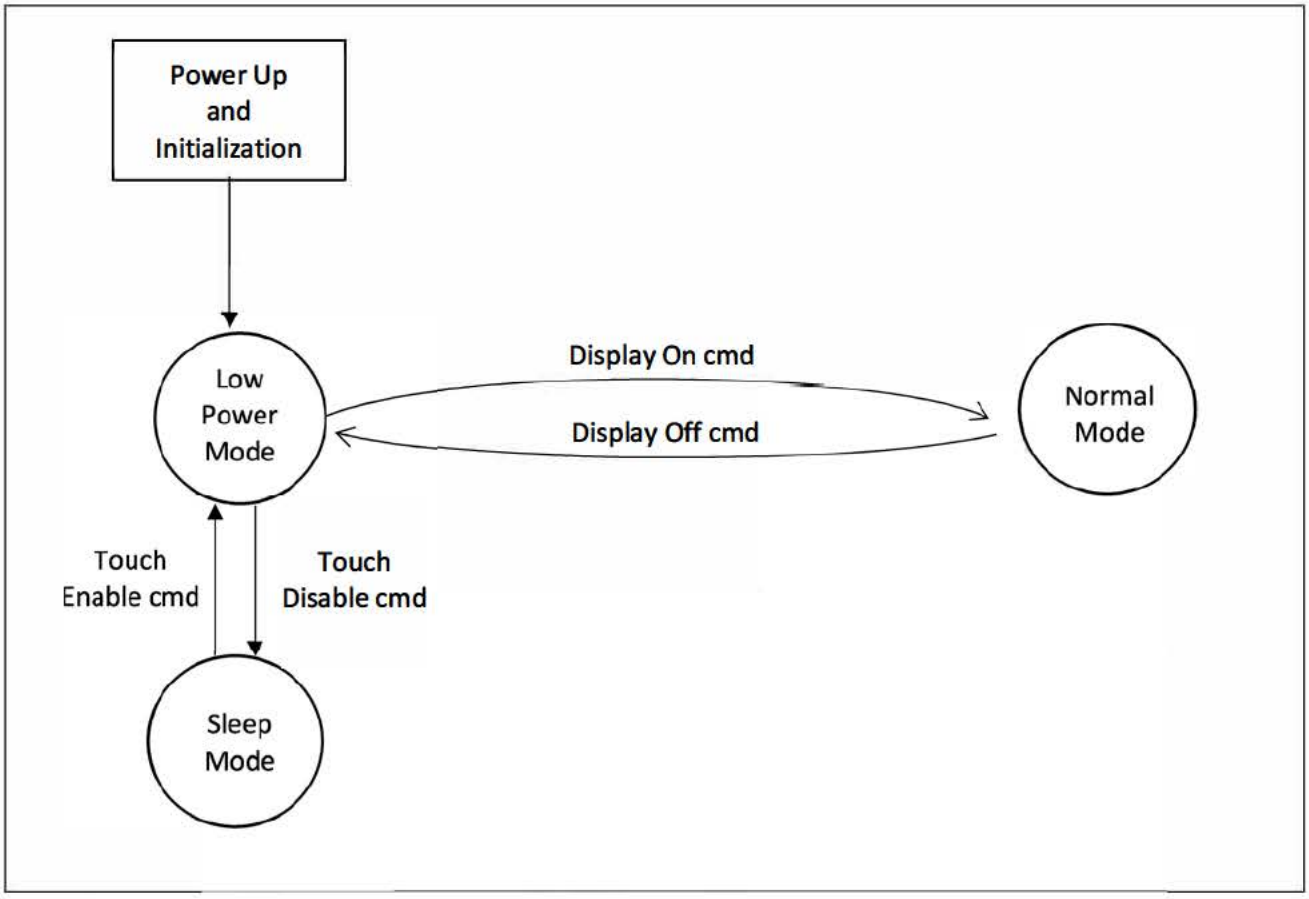
SSD7317 has integrated with 16-bit CPU, 16kB program and data memory. It is able to process all the raw touch data, generate the gesture report and communicate with the MCU host.

6.13 Touch Controller

Both TDFE and TAFE Controller is responsible for periodically generate the touch sensing period to perform touch sensing.

7 SYSTEM FLOW

Figure 7-1: Integrated Touch Controller System Flow



In Normal mode (NM), display will be on and touch scan rate will be equal to frame rate, 105Hz
In Low power mode (LPM), display will be off and touch scan rate will be equal to 20Hz, software programmable. It supports single tap, double taps and long tap wake-up gesture.

It is recommended to turn off the external DC-DC circuit for display panel driving during low power mode (LPM). In this case, V_{CC} must be higher or equivalent to $V_{CI} - 0.6V$.

In Sleep mode, touch sensing will be off. It shall respond only to the Touch enable command during the sleep mode.

8 MAXIMUM RATINGS

Table 8-1: Maximum Ratings

(Voltage Reference to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +4	V
V_{CI}		-0.3 to +4	V
V_{CC}		0 to 19	V
V_{SEG}	SEG output voltage	0 to V_{CC}	V
V_{COM}	COM output voltage	0 to 0.9*V_{CC}	V
V_{in}	Input voltage	V_{SS}-0.3 to V_{DD}+0.3	V
T_A	Operating Temperature	-40 to +8 5	℃
T_{stg}	Storage Temperature Range	-6 5 to +1 50	℃

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description.

*This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

9 DC CHARACTERISTICS

Condition (Unless otherwise specified):

Voltage referenced to V_{SS}
V_{DD} = 1.65V to 3.5V
V_{CI} = 3V to 3.5V (V_{CI} must be greater than or equal to V_{DD})
T_A = 25°C

Table 9-1: DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{CC}	Operating Voltage	-	8 (NM) V_{CI} – 0.6V (LPM)	-	18	V
V_{DD}	Logic Supply Voltage	-	1.65	-	3.5	V
V_{CI}	Touch controller Supply Voltage	-	3.0	-	3.5	V
V_{OH}	High Logic Output Level	I_{OUT} = 100uA, 3.3MHz	0.9 x V_{DD}	-	-	V
V_{OL}	Low Logic Output Level	I_{OUT} = 100uA, 3.3MHz	-	-	0.1 x V_{DD}	V
V_{IH}	High Logic Input Level	-	0.8 x V_{DD}	-	-	V
V_{IL}	Low Logic Input Level	-	-	-	0.2 x V_{DD}	V
$I_{CC, SLEEP}$	I_{CC}, Sleep mode Current	V_{DD} = 1.65V~3.5V, V_{CI} = 3V~3.5V, V_{CC} = 8V~18V Display OFF, No panel attached, No touch operation	-	-	10	uA
$I_{DD, SLEEP}$	I_{DD}, Sleep mode Current		-	-	10	uA
$I_{CI, SLEEP}$	I_{CI}, Sleep mode Current		-	-	10	uA
$I_{DD, LPM}$	I_{DD}, Low power mode Current	V_{DD} 1.8V, V_{CI} 3.3V, V_{CC} 2.7V Display OFF, No panel attached With touch operation	-	25 (20Hz) 10 (6Hz)	-	uA
$I_{CI, LPM}$	I_{CI}, Low power mode Current	LPM scan rate = 20Hz LPM scan rate = 6Hz	-	20 (20Hz) 5 (6Hz)	-	uA
$I_{CC, NM}$	V_{CC} Supply Current	V_{DD} = 1.8V, V_{CI} = 3.3V, V_{CC} = 12V, I_{REF} = 18.75uA	-	680	750	uA
$I_{CI, NM}$[(1)]	V_{CI} Supply Current	No loading, Display ON, All ON With touch operation, Normal mode	-	500	650	uA
$I_{DD, NM}$[(1)]	V_{DD} Supply Current	Contrast=FFh NM scan rate = 105Hz	-	800	1000	uA
I_{SEG}	Segment Output Current V_{DD}=1.8V, V_{CI} = 3.3V, V_{CC}=12V, I_{REF}=18.75uA, Display ON	Contrast=FFh	-	600	-	uA
		Contrast=AFh	-	412	-	
		Contrast=3Fh	-	150	-	
I_{SEG} Dev	Segment Output Current V_{DD}=1.8V, V_{CI} = 3.3V, V_{CC}=12V, I_{REF}=18.75uA, Display ON Segment output current uniformity	Dev = (I_{SEG} – I_{MID})/I_{MID} I_{MID} = (I_{MAX} + I_{MIN})/2 I_{SEG}[0:127] = Segment current at contrast = FFh	-3	-	+3	%
Adj. Dev	Adjacent pin output current uniformity (contrast = FF)	Adj Dev = (I[n]-I[n+1]) / (I[n]+I[n+1])	-2	-	+2	%

Note:
(1) $I_{CI, NM}$ and $I_{DD, NM}$ may vary under different FW version.

10 AC CHARACTERISTICS

Conditions:

Voltage referenced to V_{SS}
V_{DD} =1.65 to 3.5V
V_{CI} = 3V to 3.5V (V_{CI} must be greater than or equal to V_{DD})
T_A = 25°C

Table 10-1: AC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC}	Oscillation Frequency of Display Timing Generator	V_{DD} 1.8V	7.2	8	8.8	MHz
F_{FRM}	Frame Frequency	128x96 Graphic Display Mode, Display ON, Internal Oscillator Enabled	-	105	-	Hz
RES#	Reset low pulse width		3	-	-	us

Table 10-2: 6800-Series Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 1.65V to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	5	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	20	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	180	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	180 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 10-1: 6800-series parallel interface characteristics

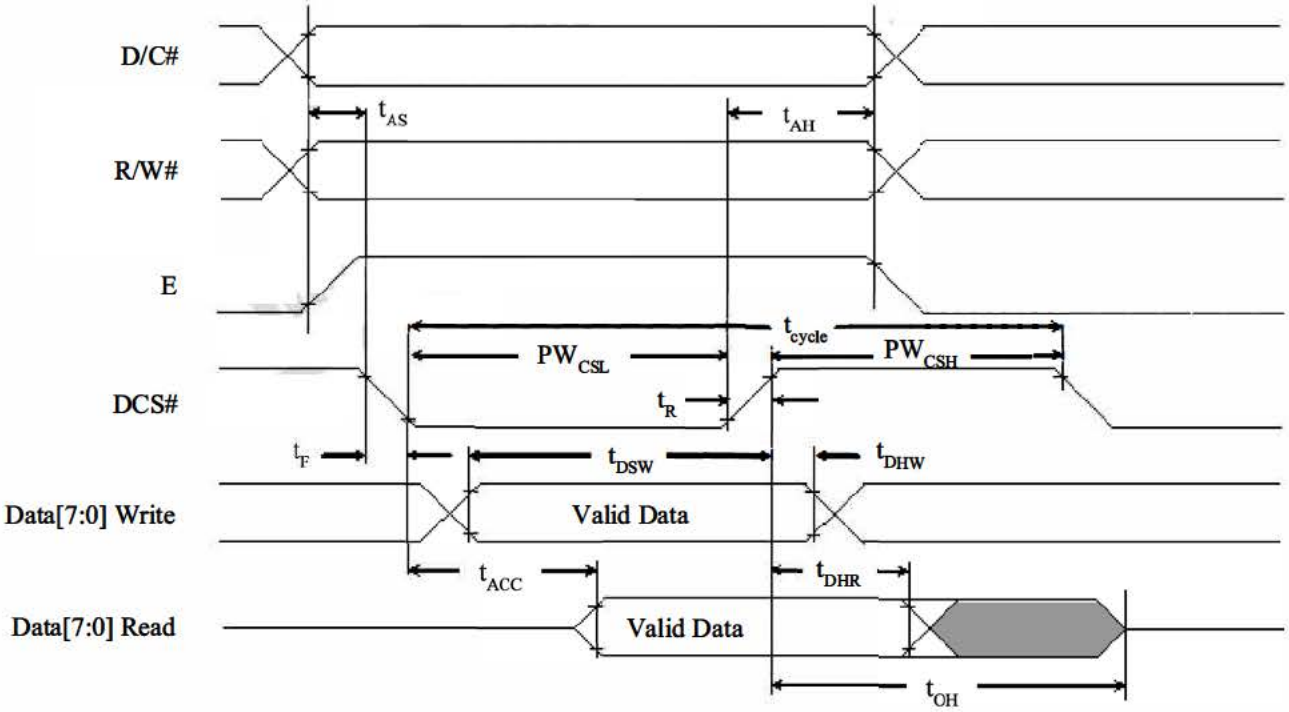
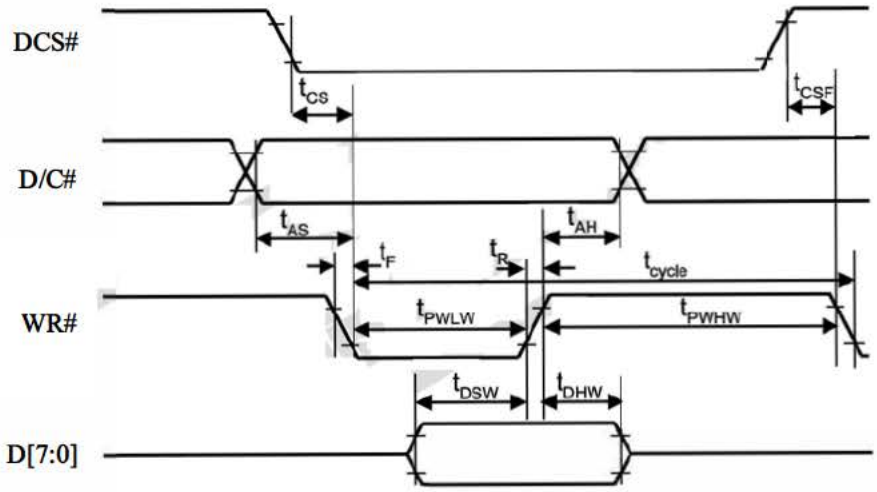


Table 10-3: 8080-Series Parallel Interface Timing Characteristics

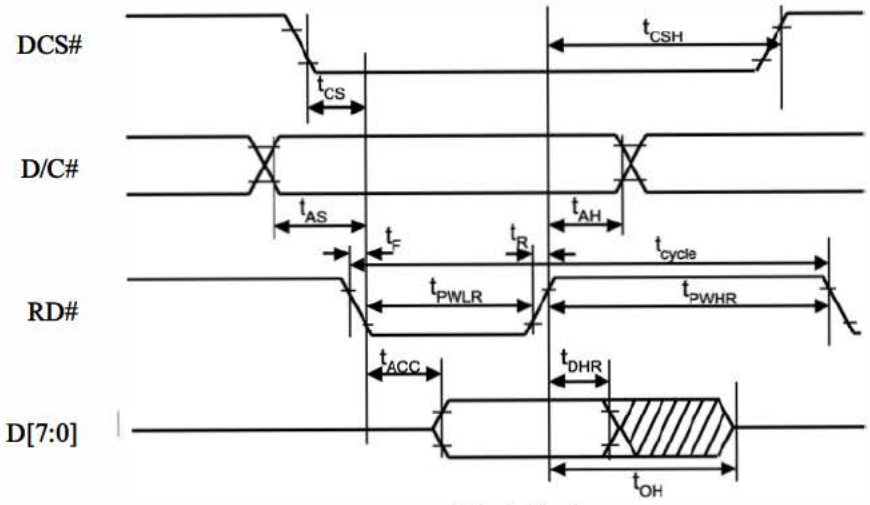
(V_{DD} - V_{SS} = 1.65V ~3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	20	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	180	ns
t_{PWLR}	Read Low Time	180	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

Figure 10-2: 8080-series parallel interface characteristics



Write Cycle



Read Cycle

Table 10-4: Serial Interface Timing Characteristics (4-wire SPI)

(V_{DD} - V_{SS} = 1.65V~3.5V, T_A = 25℃)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	20	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	25	-	-	ns
t_{CLKL}	Clock Low Time	30	-	-	ns
t_{CLKH}	Clock High Time	30	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 10-3: Serial interface characteristics (4-wire SPI)

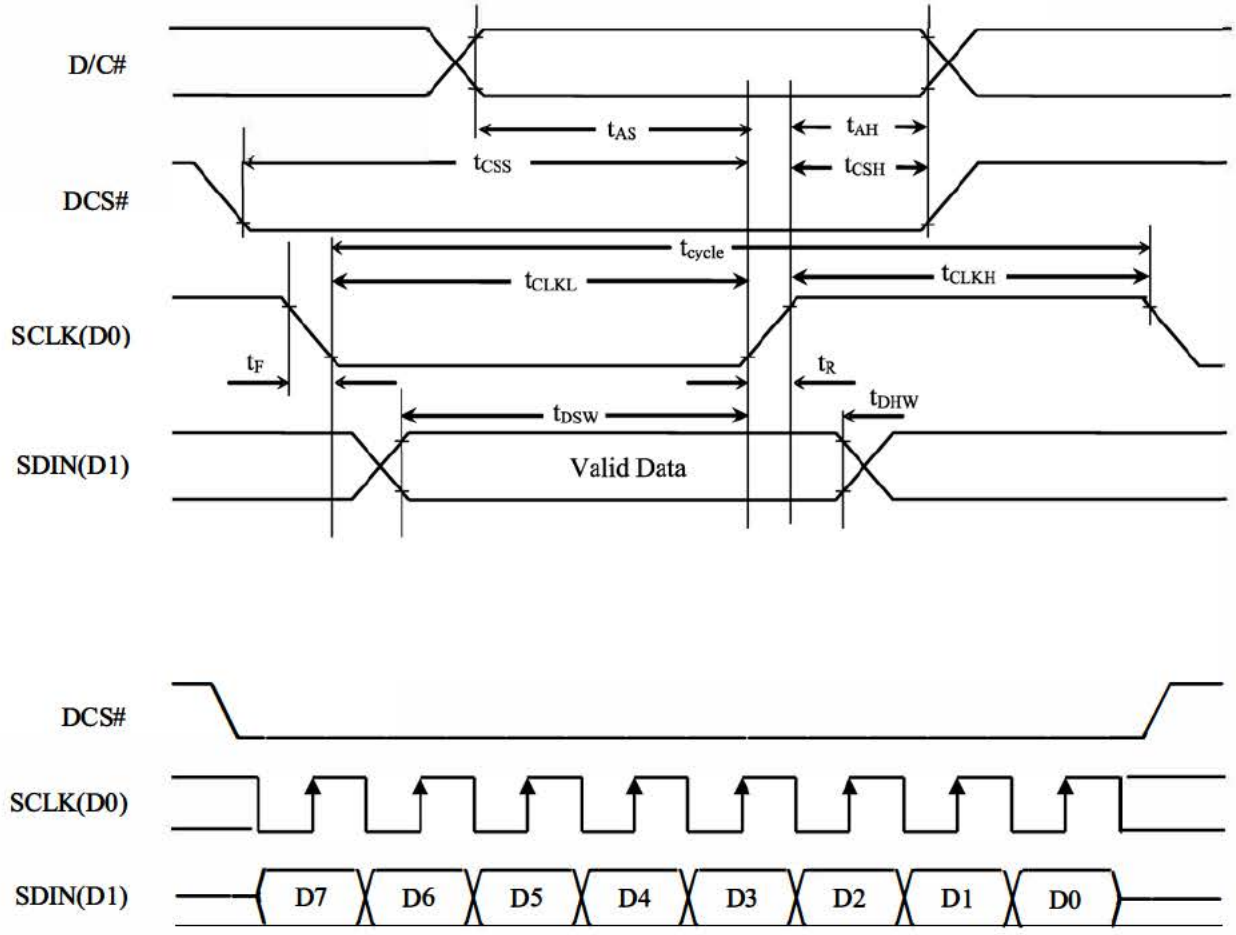


Table 10-5: Serial Interface Timing Characteristics (3-wire SPI)

(V_{DD} - V_{SS} = 1.65V~3.5V, T_A = 25℃)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	20	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	25	-	-	ns
t_{CLKL}	Clock Low Time	30	-	-	ns
t_{CLKH}	Clock High Time	30	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 10-4: Serial interface characteristics (3-wire SPI)

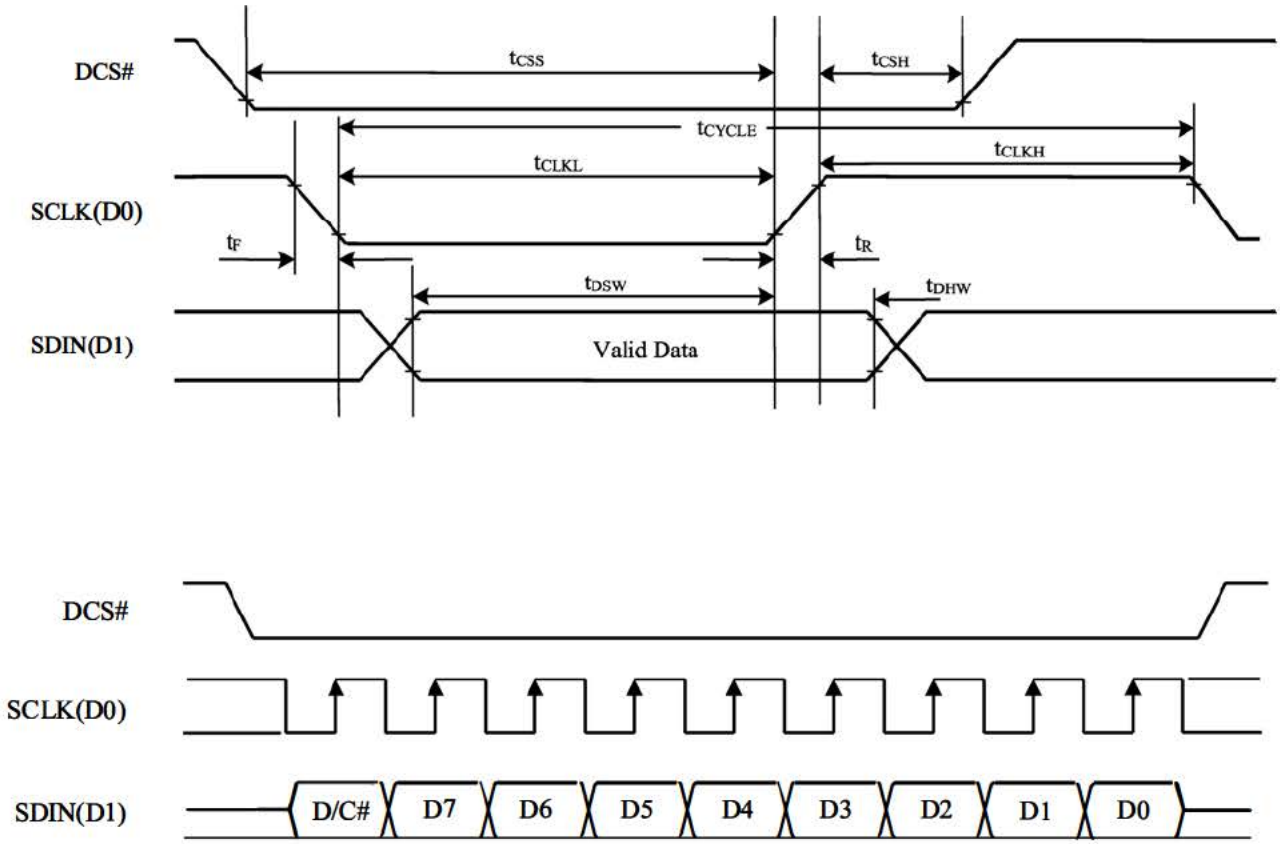
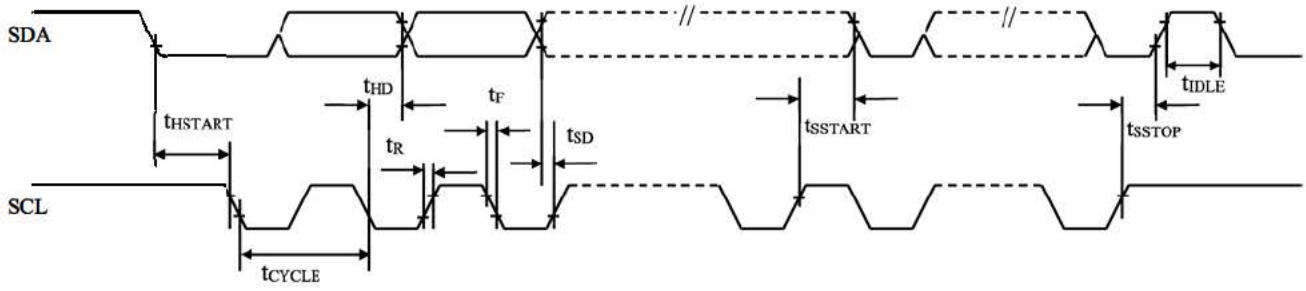


Table 10-6: I²C Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" pin)	0	-	-	ns
	Data Hold Time (for "SDA_{IN}" pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

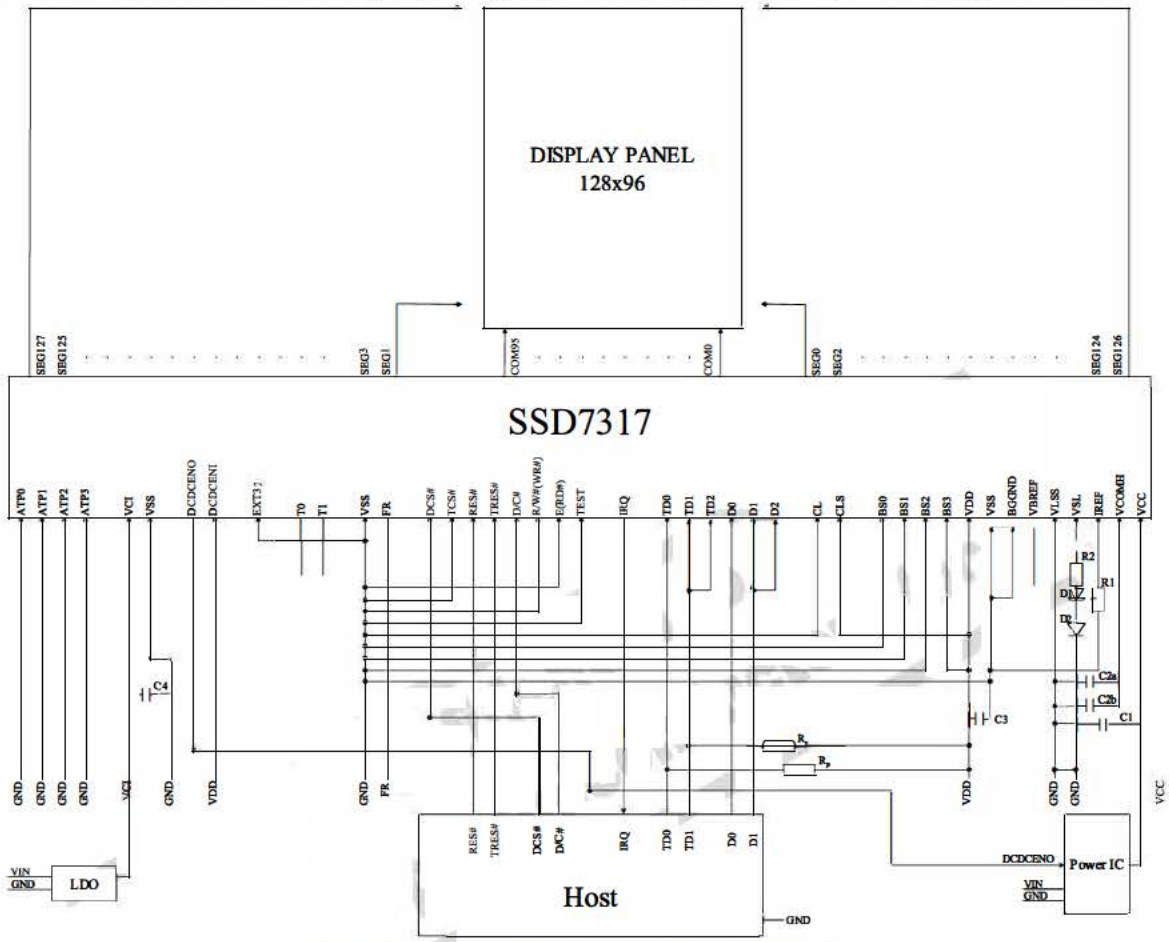
Figure 10-5: I²C interface Timing characteristics



11 APPLICATION EXAMPLE

Figure 11-1: Application Example of SSD7317 with Touch Function

The configuration for SPI4 mode to display interface, I²C mode to touch interface with 128x96 panel module application is shown in the following diagram: (V_{DD} = 1.8V, V_{CI} = 3.3V, V_{CC} = 12V, I_{REF} = 18.75uA)



Pin connected to AP interface: D[2:0], DCS#, D/C#, IRQ, TD[2:0], RES#, TRES#
Pin connected to Power IC Enable pin: DCDCENO
Pin internally connected to V_{SS}: CL, D[7:3], E, R/W#, BGGND, TCS#, EXT32, TEST
Pin internally connected to V_{DD}: CLS, DCDCENI
VBREF, FR, T0, T1, TR[19:0], RX[3:0], SHx should be left open.
ATP[3:0] should connect to external GND separately

C1, C2: 2.2uF (1)
C3, C4: 1.0uF (1)
R2, R3: Pull up resistor

Voltage at I_{REF} V_{CC} – 2V. For V_{CC} 12V, I_{REF} 18.75uA:
R1 (Voltage at I_{REF} - V_{SS}) / I_{REF}
(12-2) / 18.75uA
530KΩ

Note
(1) The capacitor value is recommended value. Select appropriate value against module application.
(2) Die gold bump face up.
(3) All V_{LSS} pads of IC are recommended to be connected together to form a larger area of GND
(4) V_{LSS} and V_{SS} are not recommended to be connected on the ITO routing, but connected together in the PCB level at one common ground point for better grounding and noise insulation.

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The product(s) listed in this datasheet comply with Directive (EU) 2015/863 of 31 March 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances and People's Republic of China Electronic Industry Standard GB/T 26572 2011 "Requirements for concentration limits for certain hazardous substances in electronic information products (电子电器产品中限用物質的限用要求)". Hazardous Substances test report is available upon request.

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SSD7317

SPI Software Porting User Guide

Revision history of SSD7317 SPI Software Porting User Guide

Version	Change Items	Effective Date
0.1	1st Release	2-Jan-19
1.0	Update guideline to support FW6.x	30-Apr-19

CONTENTS

1. SPI Operation Format

1.1. Notes

1. CPOL 0, CPHA 0
2. All command, address, data are 16-bit width
3. Byte Order: In most cases, LSB comes first and then MSB comes. **
4. Bit Order: In all cases, most significant bit comes first.
5. Different read/write operation in BIOS and CPU mode

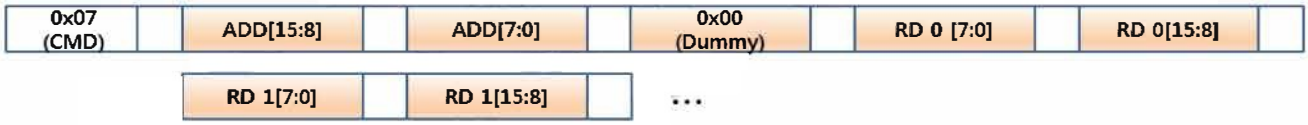
1.2. BIOS mode

1.2.1. Register Write Operation

1.2.2. Register Read Operation

1.2.3. Data Burst Write Operation

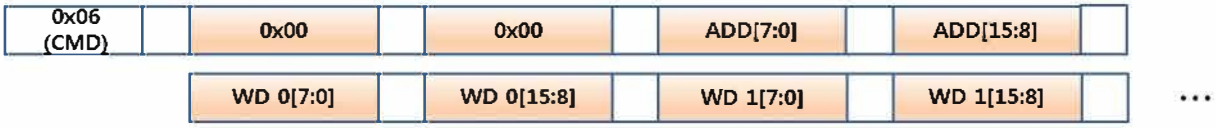
1.2.4. Data Burst Read Operation



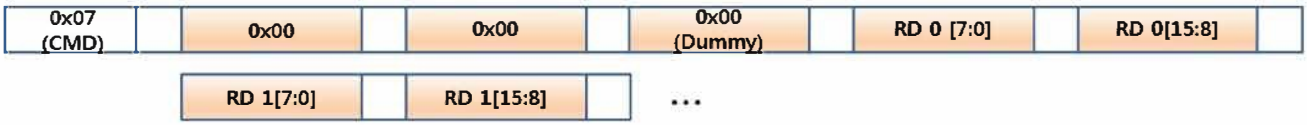
1.3. CPU mode

1.3.1. Register Read Operation

1.3.2. Data Burst Write Operation



1.3.3. Data Burst Read Operation



2. Data Definition

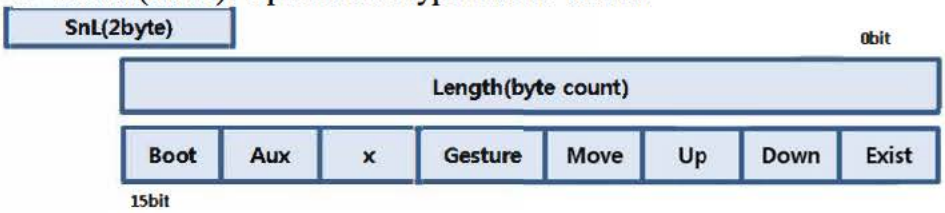
2.1. SPI_CTRL_ST

1. Status Register

Bit	Name	Description
15	INT_RST	Set : Interrupt by HW reset
14	OSC_EN	Set : OSC Enable
13	CRC_BSY	Set : CRC busy
12:1	X	x
0	SPIS_BUSY	Set : SPIS busy

2.2. SnL: Status and Length

1. Address: 0x0AF0
2. Length(LSB): Bytes of upload data to read.
3. Status(MSB): Upload data type and IC Status



2.3. Gesture Upload Data

1. Address: 0x0AF1
2. 6-byte upload data for recognized gesture

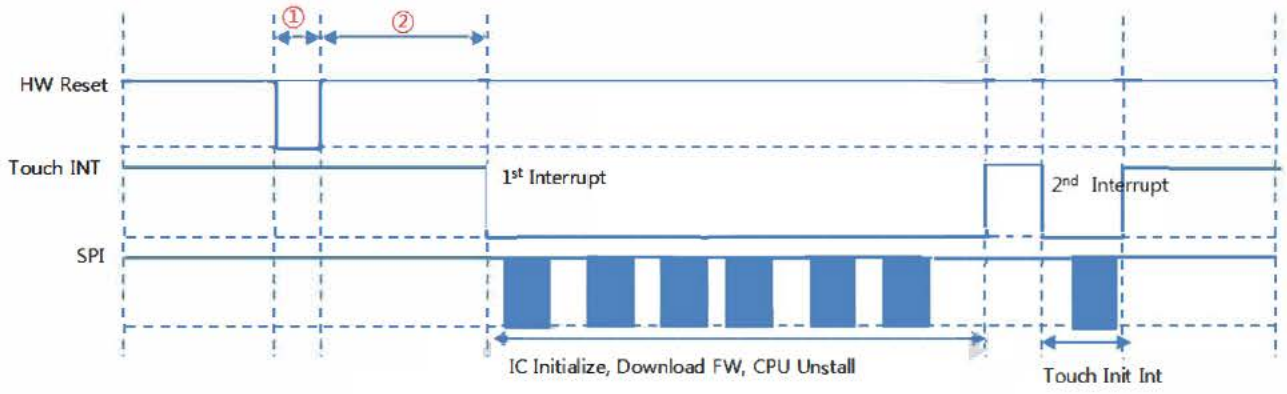
	7	6	5	4	3	2	1	0
Byte 0	Gesture(8bit : 0xF6)							
Byte 1	Gesture ACT							
Byte 2	Gesture Detail							
Byte 3	Tap Down Key						Tap Up Key	
Byte 4	Reserved							
Byte 5	Reserved						Slide Direction ID	

Name	Gesture ACT	Gesture Detail	Down/Up Key position		Direction ID	Action Description	Mode Support
			Tap Down Key	Tap Up Key			
Single Tap Key1	0x01	0x01	x	x		D U	NM
Single Tap Key2	0x01	0x02	x	x		D U	NM
Single Tap Key3	0x01	0x03	x	x		D U	NM
Single Tap Key4	0x01	0x04	x	x		D U	NM
Single Tap AnyKey	0x01	0x00	x	x		D U	NM, LPM
Long Tap Key1	0x02	0x01	x	x		D Delay U	NM
Long Tap Key2	0x02	0x02	x	x		D Delay U	NM
Long Tap Key3	0x02	0x03	x	x		D Delay U	NM
Long Tap Key4	0x02	0x04	x	x		D Delay U	NM
Long Tap AnyKey	0x02	0x00	x	x		D Delay U	NM, LPM
Double Tap Key1	0x03	0x01	x	x		D U D U	NM
Double Tap Key2	0x03	0x02	x	x		D U D U	NM
Double Tap Key3	0x03	0x03	x	x		D U D U	NM
Double Tap Key4	0x03	0x04	x	x		D U D U	NM
Double Tap AnyKey	0x03	0x00	x	x		D U D U	NM, LPM
Slide LR or TB	0x04	0x01	[6:4] Key Num	[2:0] Key Num	X: 1, Y: 2, External Key: 3	D Move U	NM
Slide RL or BT	0x04	0x02	[6:4] Key Num	[2:0] Key Num	X: 1, Y: 2, External Key: 3	D Move U	NM
Error	0xFF	0x00	x	x		Time out / Palm/etc	NM, LPM

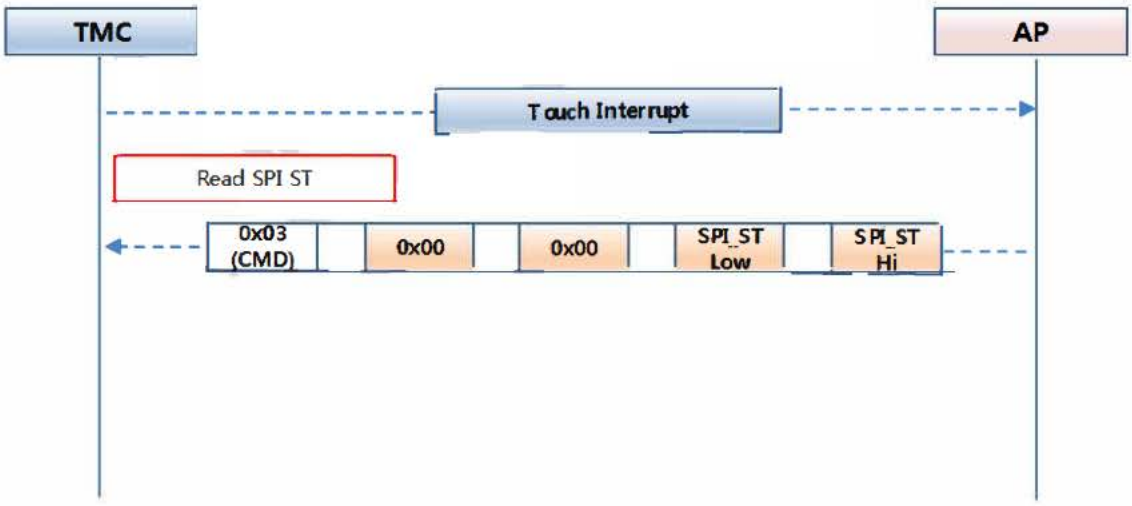
3. Reset and Boot

3.1. Steps

1. Display and Touch initial code
   1.1 Touch initial code with 0x35 set to 0x10
2. ① : Touch HW Reset to Low > 10us
3. ② : HW reset to BIOS Reset Interrupt expected > 20ms
4. 1st Interrupt: BIOS Reset Interrupt.
   4.1 IC Initialize
   4.2 Download FW
   4.3 CPU Unstall : enter CPU mode after IC Initialize
5. 2nd Interrupt : Touch initialize Interrupt
   5.1 Issue Clear Interrupt command



3.2. IC Initialization



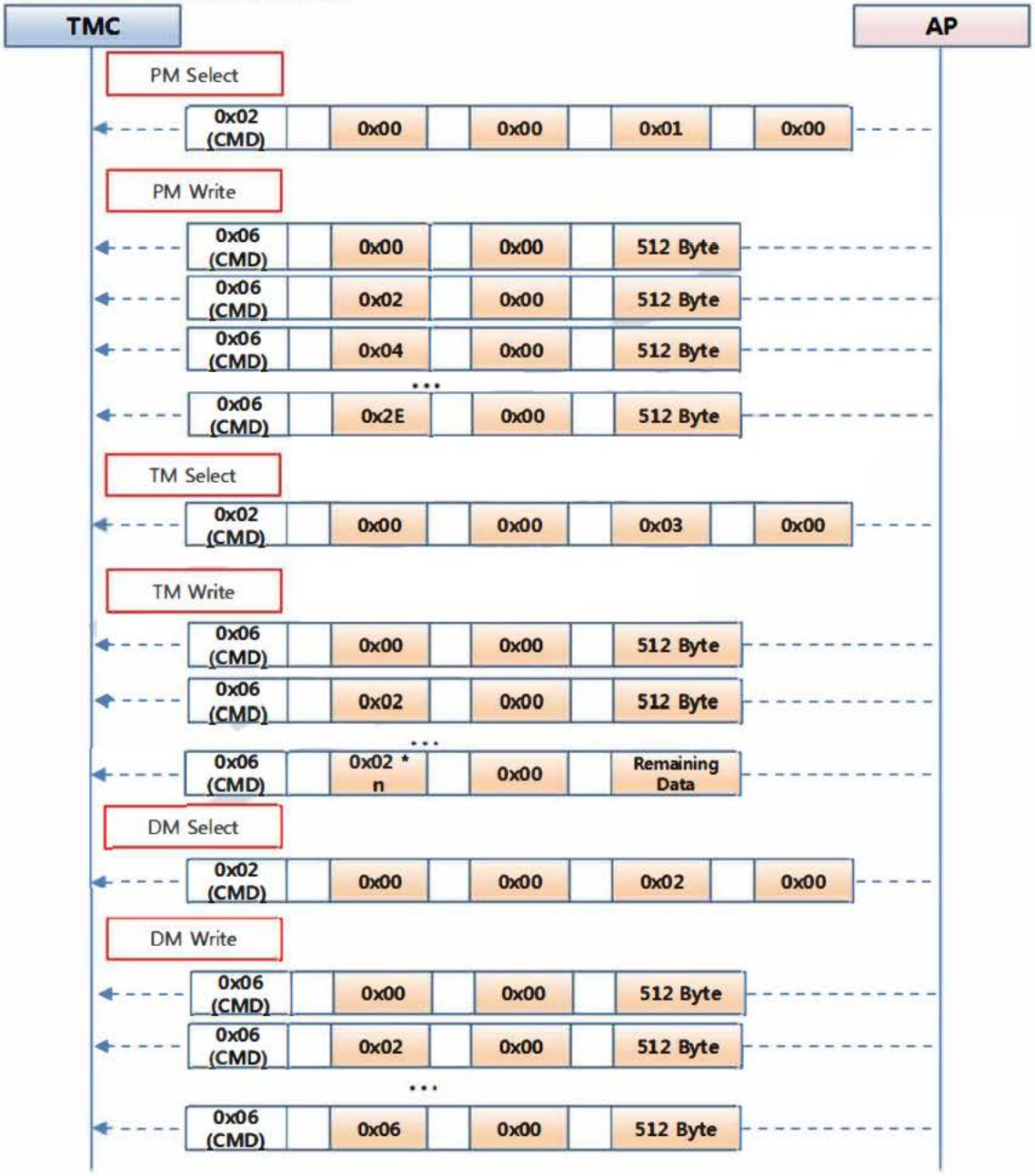
3.3. FW Download

3.3.1. SSD7317 has 16K ram size which is divided into 3 blocks. PM is 12K bytes, DM is 2K bytes and PM is 2K bytes.

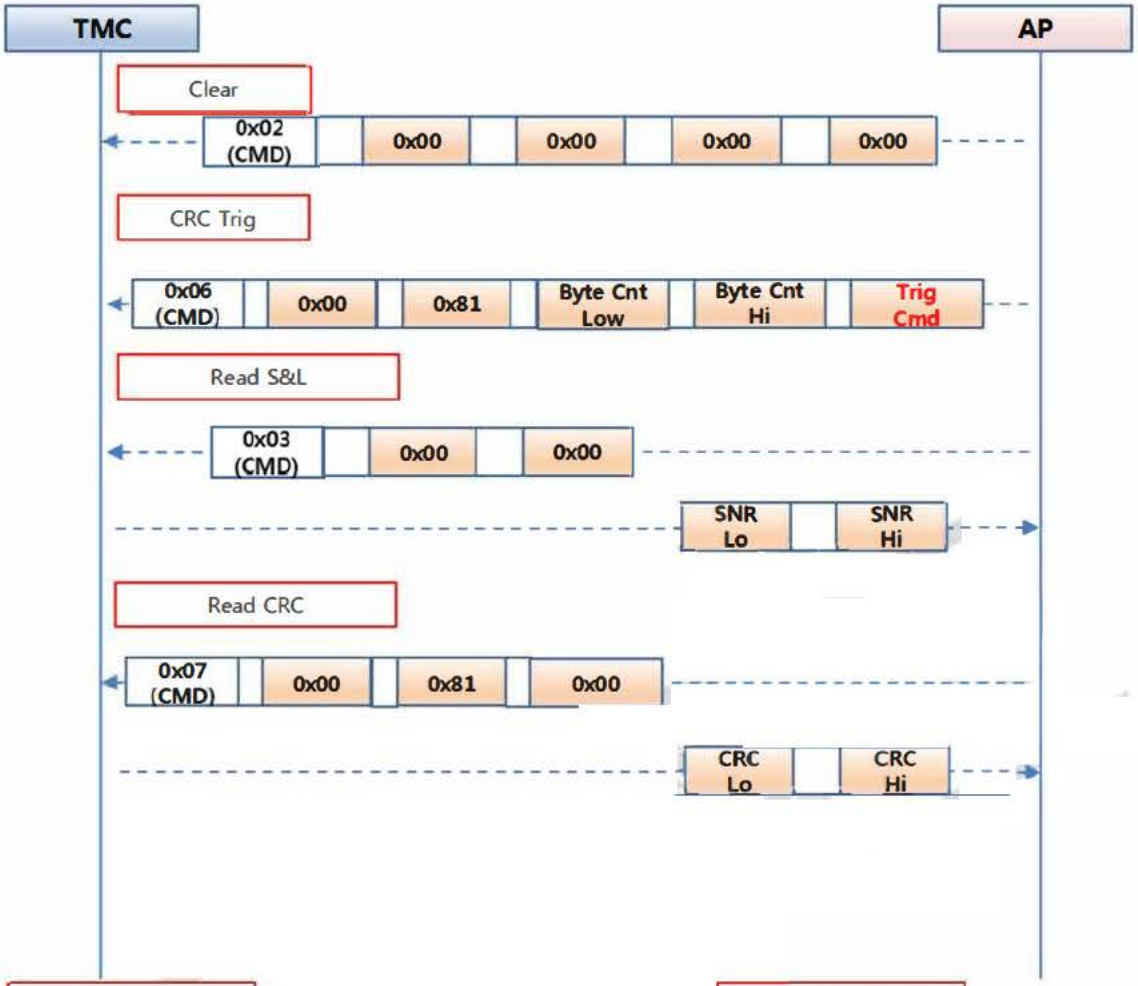
3.3.2. FW header file contains 3 code blocks

1. PM_Content
2. TM_Content
3. DM_Content

3.3.3. FW download flow



3.3.4. CRC Checksum



S&L

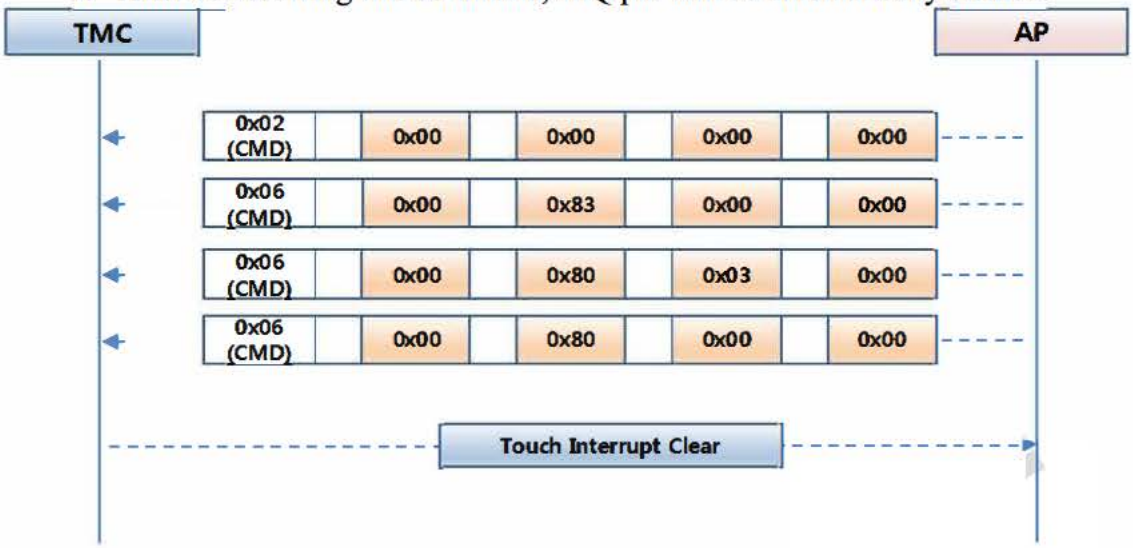
Bit	Name	RD(2byte)
15	INT_RST	Set : Interrupt by HW reset
14	OSC_EN	Set : OSC Enable
13	CRC_BSY	Set : CRC busy
12:1	X	x
0	SPIS_BUSY	Set : SPIS busy

Trig Cmd

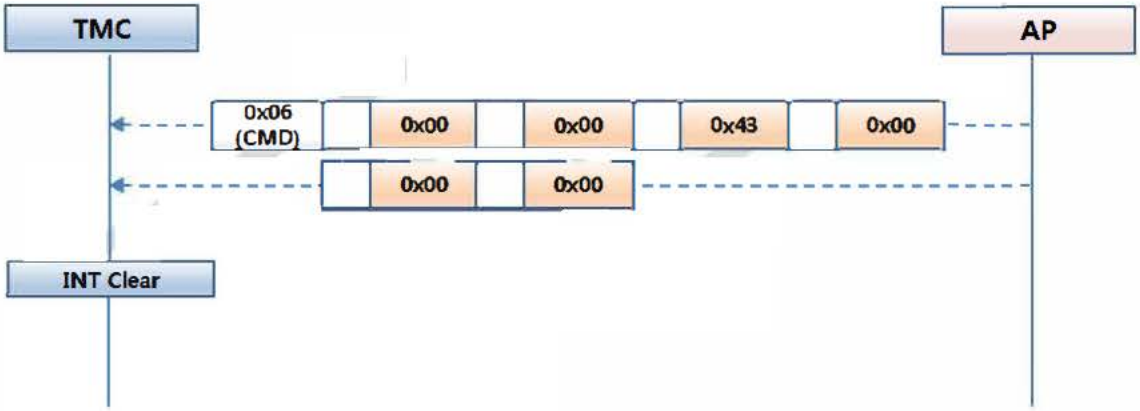
Memory Select	WD(2byte)
PM Select	0x01
TM Select	0x03
DM Select	0x02

3.3.5. CPU Unstall

1. After IC receiving this command, IRQ pin will be automatically cleared.

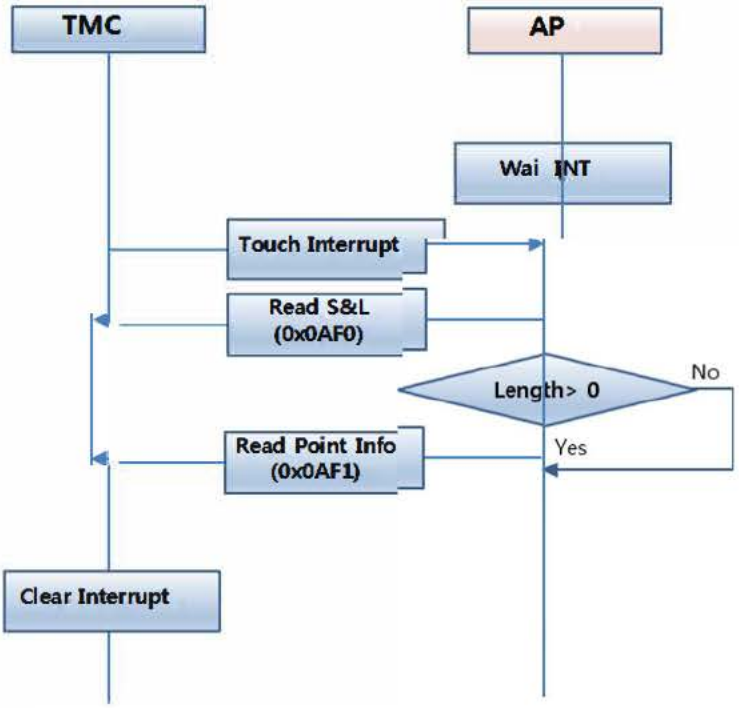


3.3.6. Clear Interrupt

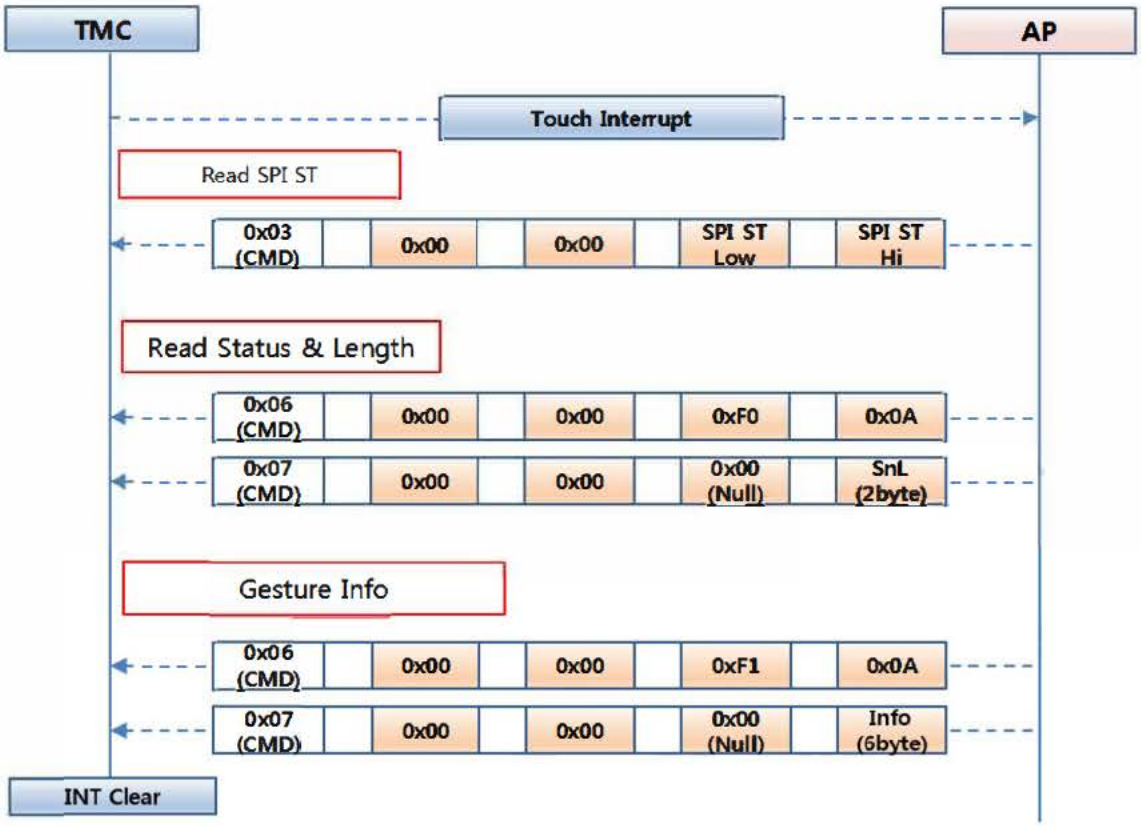


4. Touch Event Reading

4.1. Event Flow



4.2. Command Flow



SSD7317

I²C Software Porting User Guide

Revision history of SSD7317 I²C Software Porting User Guide

Version	Change Items	Effective Date
0.1	1st Release	17-Dec-18
1.0	Update guideline to support FW6.x	30-Apr-19
1.1	Update the table in 2.2 Gesture data Update 3.1 Steps for Reset and Boot Revise the figures of Section 3.3 FW Download Add 5 Display off sequence from NM to LPM	2-Aug-19

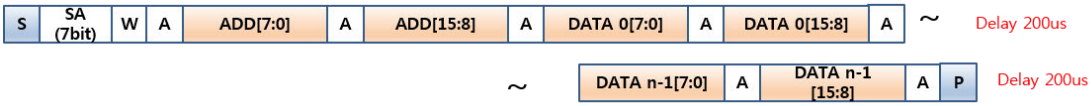
CONTENTS

1. *I2C Operation Format*

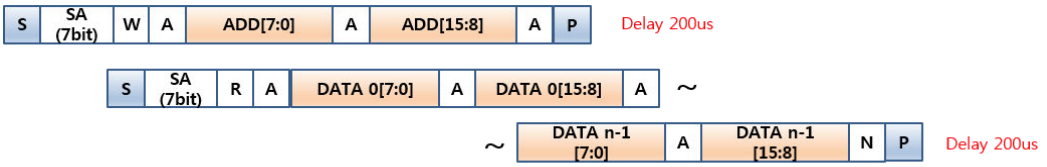
1.1. Notes

1. Two 7-bit Slave Address
1.1 Touch init command 0x35 set to 0x0A: SA with 0x53 and SA BIOS with 0x57
1.2 Touch init command 0x35 set to 0x0B: SA with 0x5B and SA BIOS with 0x5F
2. All command, address, data are 16-bit width
3. Byte Order: In most cases, LSB comes first and then MSB comes. **
4. Bit Order: In all cases, most significant bit comes first.
5. Need to Packet Delay 200us

1.2. Write Operation



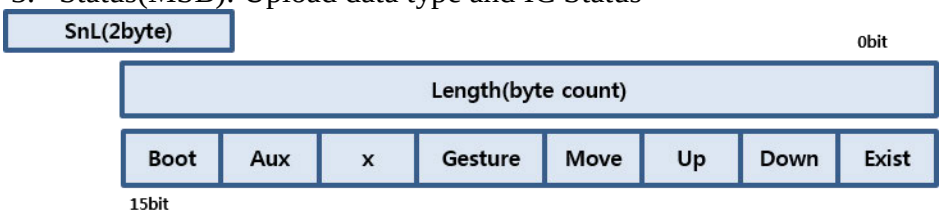
1.3. Read Operation



2. *Register Map Definition*

2.1. SnL: Status and Length

1. Register Address: 0x0AF0
2. Length(LSB): Bytes of upload data to read.
3. Status(MSB): Upload data type and IC Status



2.2. Gesture Upload Data

1. Register Address: 0x0AF1
2. 6-byte upload data for recognized gesture

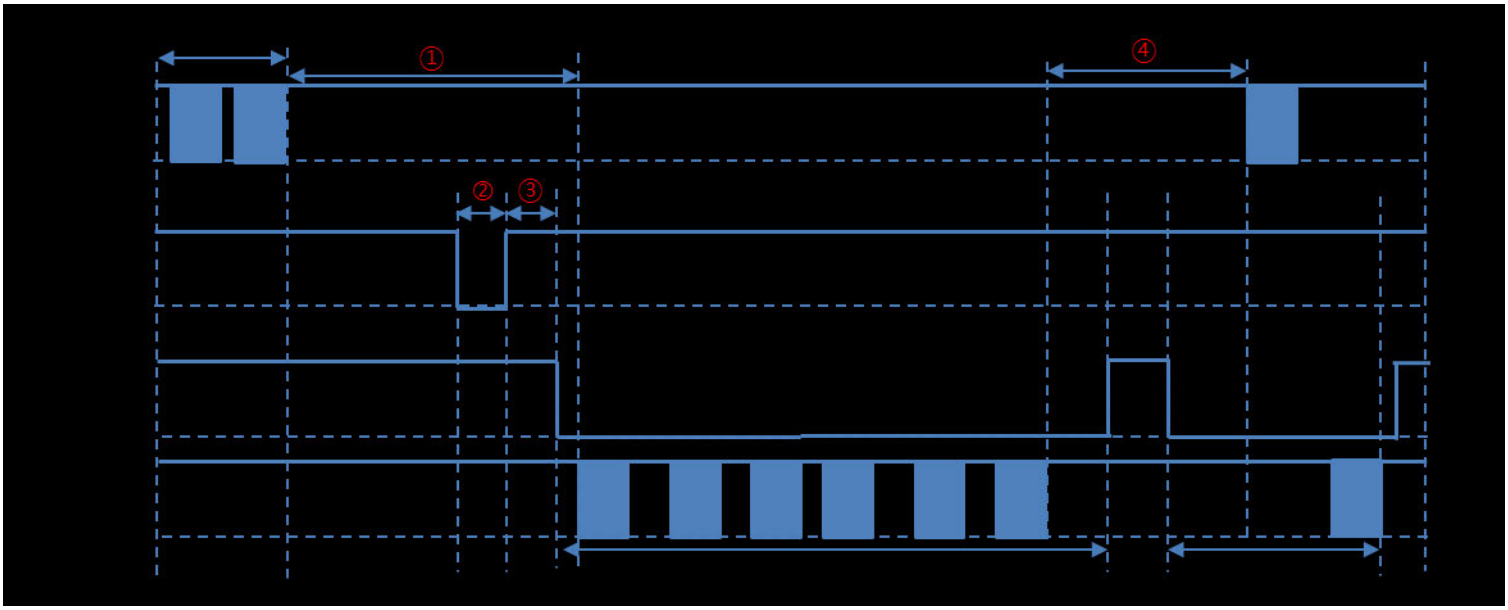
	7	6	5	4	3	2	1	0
Byte 0	Gesture(8bit : 0xF6)							
Byte 1	Gesture ACT							
Byte 2	Gesture Detail							
Byte 3		Tap Down Key				Tap Up Key		
Byte 4	Reserved							
Byte 5	Reserved				Slide Direction ID			

Name	Gesture ACT	Gesture Detail	Down/Up Key position		Direction ID	Action Description	Mode Support
			Tap Down Key	Tap Up Key			
Single Tap Key1	0x01	0x01	x	x	Internal Key: 1, External Key: 3	D-U	NM
Single Tap Key2	0x01	0x02	x	x		D-U	NM
Single Tap Key3	0x01	0x03	x	x		D-U	NM
Single Tap Key4	0x01	0x04	x	x		D-U	NM
Single Tap AnyKey	0x01	0x00	x	x		D-U	NM, LPM
Long Tap Key1	0x02	0x01	x	x	Internal Key: 1, External Key: 3	D-Delay-U	NM
Long Tap Key2	0x02	0x02	x	x		D-Delay-U	NM
Long Tap Key3	0x02	0x03	x	x		D-Delay-U	NM
Long Tap Key4	0x02	0x04	x	x		D-Delay-U	NM
Long Tap AnyKey	0x02	0x00	x	x		D-Delay-U	NM, LPM
Double Tap Key1	0x03	0x01	x	x	Internal Key: 1, External Key: 3	D-U-D-U	NM
Double Tap Key2	0x03	0x02	x	x		D-U-D-U	NM
Double Tap Key3	0x03	0x03	x	x		D-U-D-U	NM
Double Tap Key4	0x03	0x04	x	x		D-U-D-U	NM
Double Tap AnyKey	0x03	0x00	X	x		D-U-D-U	NM, LPM
Slide LR	0x04	0x01	[6:4] Key Num	[2:0] Key Num	X: 1, Y: 2 External Key: 3	D-Move-U	NM
Slide RL	0x04	0x02	[6:4] Key Num	[2:0] Key Num	X: 1, Y: 2 External Key: 3	D-Move-U	NM
Error	0xFF	0x00	x	x		Time out / Palm/etc	NM, LPM

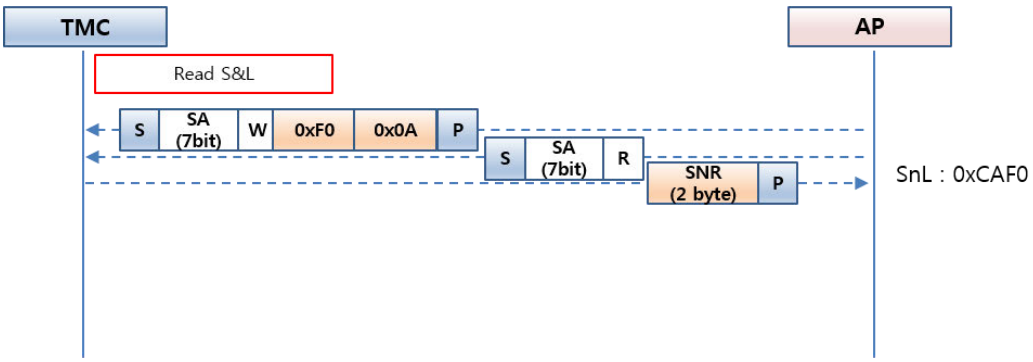
3. *Reset and Boot*

3.1. Steps

1. Display and Touch initial code
2. ① : Wait 20ms before touch command initialization
3. ② : Touch HW Reset to Low > 10us
4. ③ : HW reset to BIOS Reset Interrupt expected > 10us
5. 1st Interrupt : BIOS Reset Interrupt
   - 5.1 IC Initialize
   - 5.2 Download FW
   - 5.3 CPU Unstall : enter CPU mode after IC Initialize
6. After CPU Unstall, ④ : wait > 5ms and send display command 0xF4, 0x90 for initialization complete.
7. 2nd Interrupt : Touch initialize Interrupt
   - 7.1 Issue Clear Interrupt command



3.2. IC Initialization



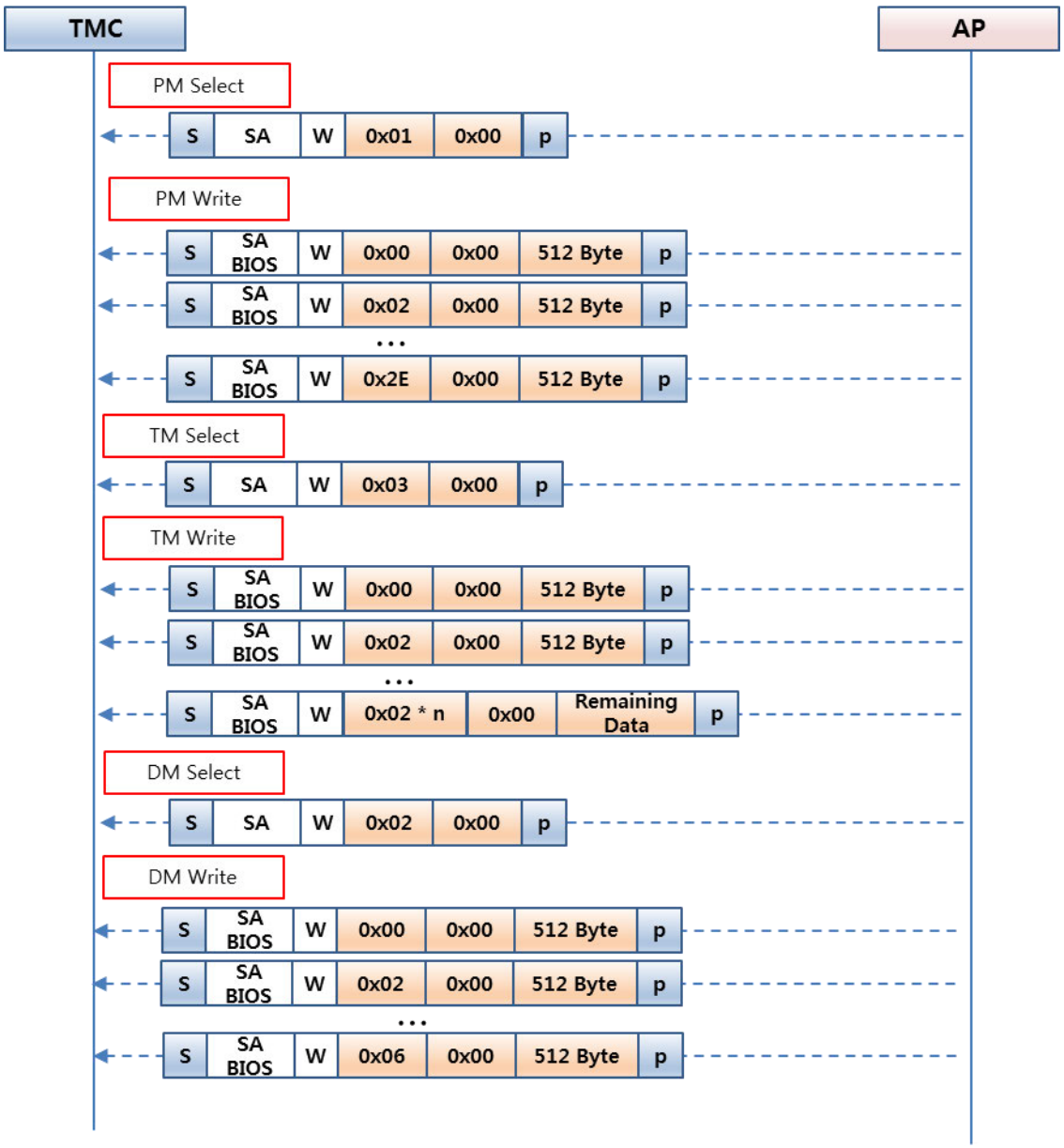
3.3. FW Download

3.3.1. SSD7317 has 16K ram size which is divided into 3 blocks. PM is 12K bytes, DM is 2K bytes and PM is 2K bytes.

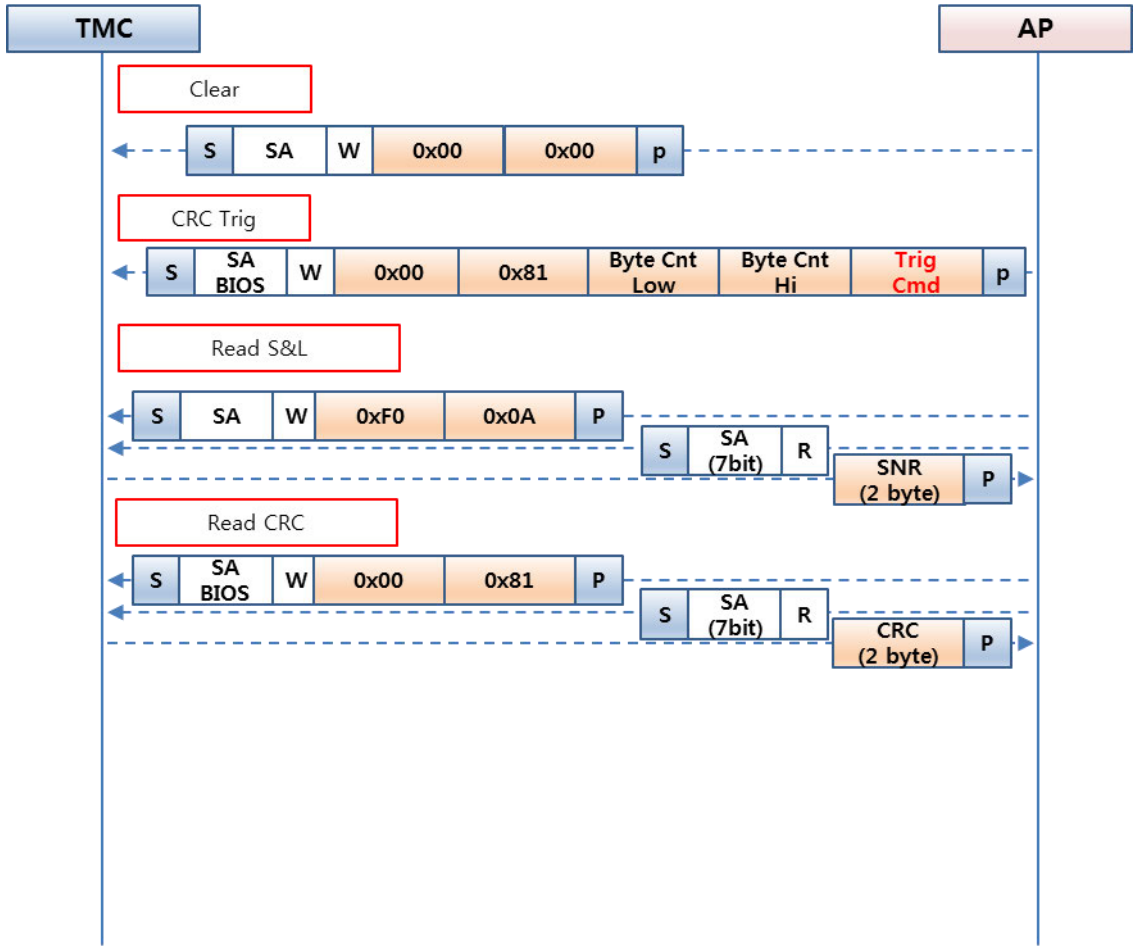
3.3.2. FW header file contains 3 code blocks

1. PM_Content
2. TM_Content
3. DM_Content

3.3.3. FW download flow



3.3.4. CRC Checksum



S&L

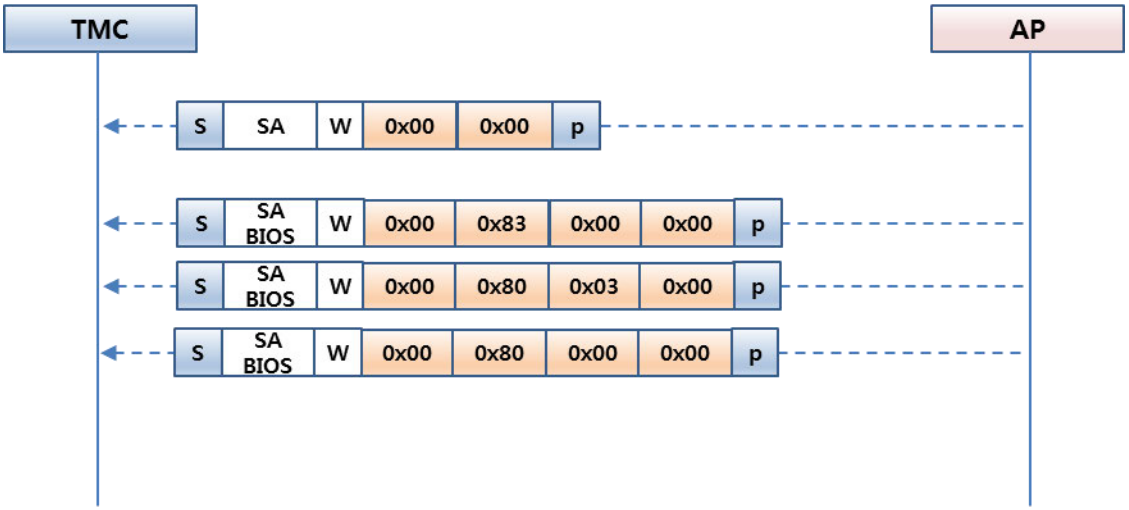
Bit	Name	RD(2byte)
15	INT_RST	Set : Interrupt by HW reset
14	OSC_EN	Set : OSC Enable
13	CRC_BSY	Set : CRC busy
12:0	X	x

Trig Cmd

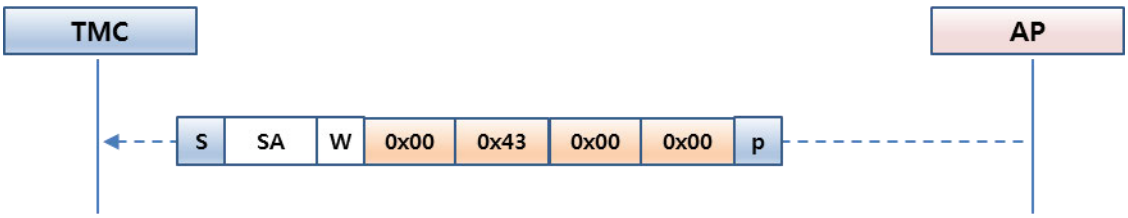
	Name	RD(2byte)
	0x03	PM Trig
	0x05	DM Trig
	0x09	TM Trig

3.3.5. CPU Unstall

1. After IC receiving this command, IRQ pin will be automatically cleared.

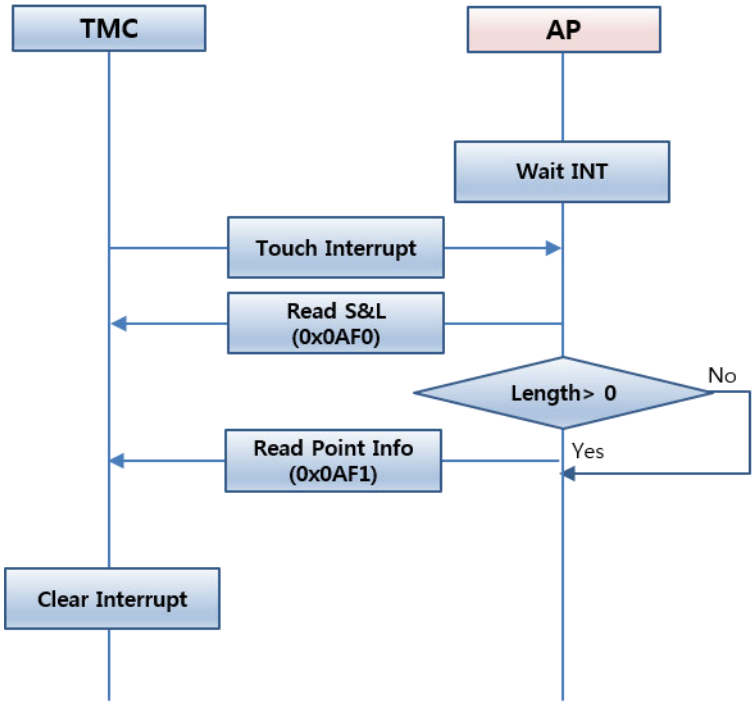


3.3.6. Clear Interrupt

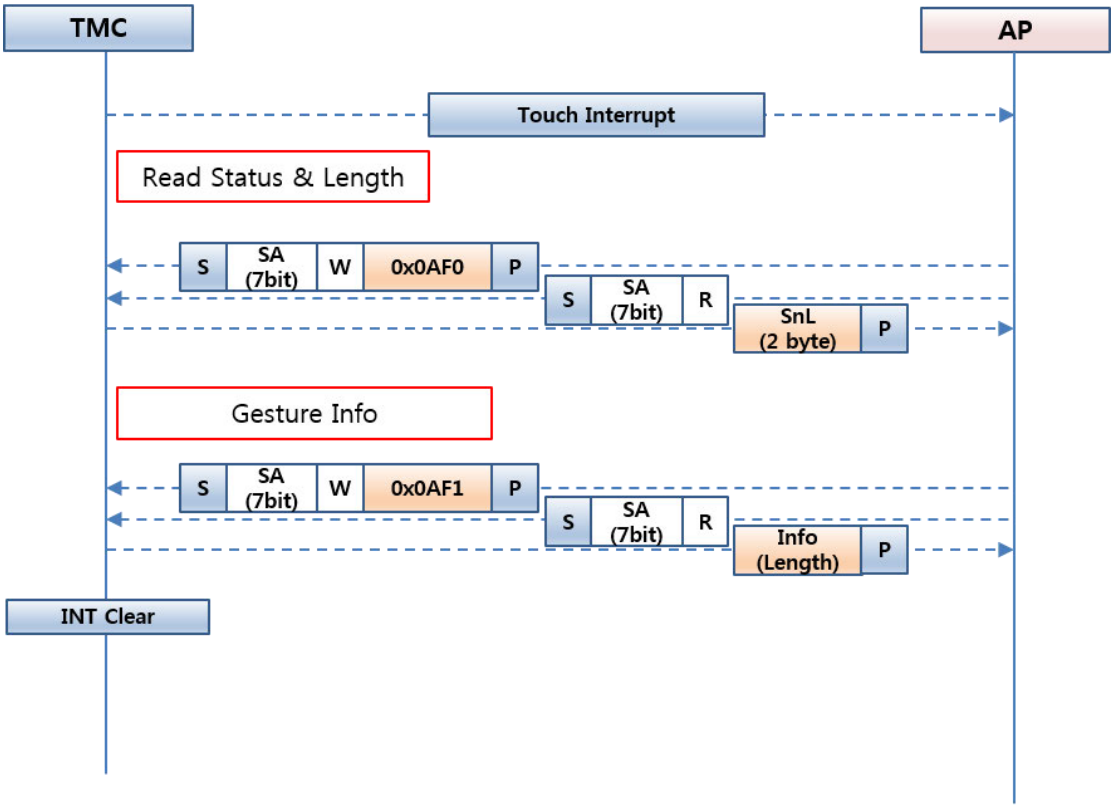


4. *Touch Event Reading*

4.1. Event Flow



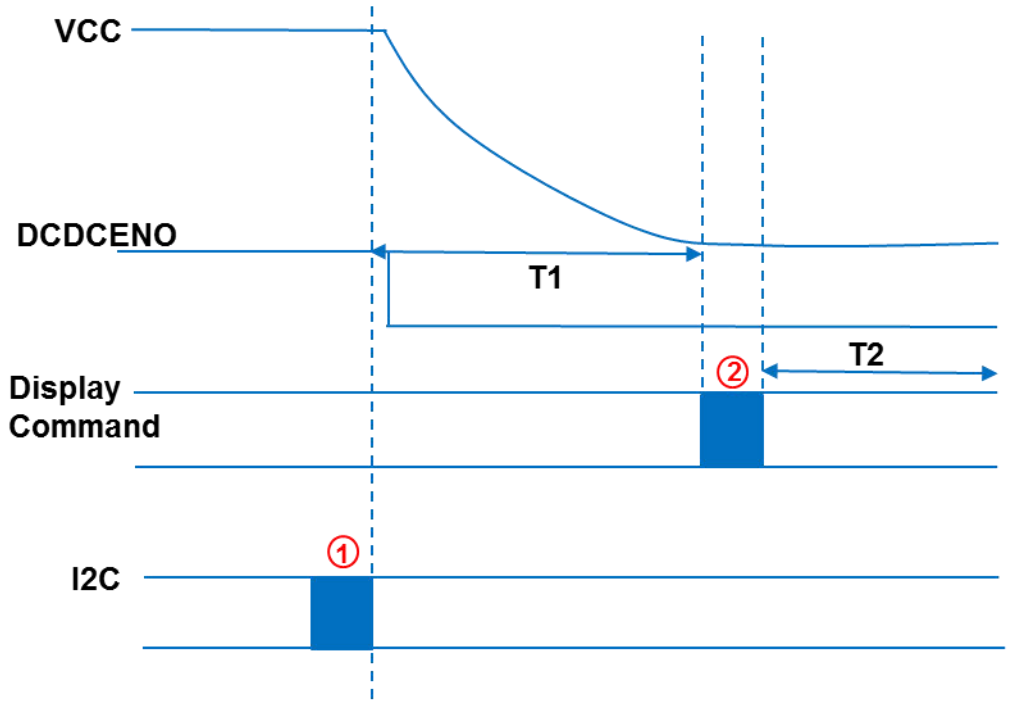
4.2. Command Flow



5. *Display Off Sequence*

5.1. Normal Mode (NM) to Low Power Mode (LPM)

Send ① touch off command 0x37, 0x00, 0x01, 0x00 by I2C. DCDCENO will be logic low and V_{CC} begins to discharge.
V_{CC} turns off after T1 (typ=150ms), then send ② display off command (0xAE) to the IC. SSD7317 enters LPM after T2 (typ=250ms).



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APPENDIX SUMMARY

Reference	Item
APPENDIX I	SSD7317 Bump Die Pad Coordinates
APPENDIX II	SSD7317Z Die Pad Floor Plan
APPENDIX III	SSD7317 Command Table and Command Descriptions
APPENDIX IV	SSD7317Z Die Tray Information

A pendix I: SSD7317 Bump Die Pad Coordinates

Table 1 : SSD7317 Bump Die Pad Coordinates

Pin no.	Pin nam	x	y
1	NC	-4345	-505.5
2	DR0	-4290	-505.5
3	DR1	-4235	-505.5
4	NC	-4180	-505.5
5	ATP0	-4125	-505.5
6	ATP1	-4070	-505.5
7	ATP2	-4015	-505.5
8	ATP3	-3960	-505.5
9	SHA	-3905	-505.5
10	RX0	-3850	-505.5
11	RX1	-3795	-505.5
12	RX2	-3740	-505.5
13	RX3	-3685	-505.5
14	SHB	-3630	-505.5
15	VCI	-3575	-505.5
16	VCI	-3520	-505.5
17	VSS	-3465	-505.5
18	VSS	-3410	-505.5
19	NC	-3355	-505.5
20	VCC	-3300	-505.5
21	VCC	-3245	-505.5
22	VCC	-3190	-505.5
23	VCC	-3135	-505.5
24	VCC	-3080	-505.5
25	VCOMH	-3025	-505.5
26	VCOMH	-2970	-505.5
27	VCOMH	-2915	-505.5
28	VCOMH	-2860	-505.5
29	VSL	-2805	-505.5
30	VSL	-2750	-505.5
31	VLSS	-2695	-505.5
32	VLSS	-2640	-505.5
33	VLSS	-2585	-505.5
34	VLSS	-2530	-505.5
35	VLSS	-2475	-505.5
36	DCDCENO	-2420	-505.5
37	DCDCENI	-2365	-505.5
38	VDD	-2310	-505.5
39	VDD	-2255	-505.5
40	EXT32	-2200	-505.5
41	VLL	-2145	-505.5
42	T0	-2090	-505.5
43	VLH	-2035	-505.5
44	T1	-1980	-505.5
45	VSS	-1925	-505.5
46	VSS	-1870	-505.5
47	FR	-1815	-505.5
48	VLL	-1760	-505.5
49	DCS#	-1705	-505.5
50	TCS#	-1650	-505.5
51	RES#	-1595	-505.5
52	TRES#	-1540	-505.5
53	D/C#	-1485	-505.5
54	VLL	-1430	-505.5
55	R/W#(WR#)	-1375	-505.5
56	E(RD#)	-1320	-505.5
57	TEST	-1265	-505.5
58	IRQ	-1210	-505.5
59	VDD	-1155	-505.5
60	VDD	-1100	-505.5
61	TD0	-1045	-505.5
62	TD1	-990	-505.5
63	TD2	-935	-505.5
64	D0	-880	-505.5
65	D1	-825	-505.5
66	D2	-770	-505.5
67	D3	-715	-505.5
68	VLL	-660	-505.5
69	D4	-605	-505.5
70	D5	-550	-505.5
71	D6	-495	-505.5
72	D7	-440	-505.5
73	CL	-385	-505.5
74	VLL	-330	-505.5
75	CLS	-275	-505.5
76	VLH	-220	-505.5
77	VLH	-165	-505.5
78	BS0	-110	-505.5
79	VLL	-55	-505.5
80	BS1	0	-505.5
81	VLH	55	-505.5
82	BS2	110	-505.5
83	VLL	165	-505.5
84	BS3	220	-505.5
85	VLH	275	-505.5
86	VDD	330	-505.5
87	VDD	385	-505.5
88	VDD	440	-505.5
89	VSS	495	-505.5
90	VSS	550	-505.5
91	VSS	605	-505.5
92	VSS	660	-505.5
93	BGGND	715	-505.5
94	VBREF	770	-505.5
95	VLSS	825	-505.5
96	VLSS	880	-505.5
97	VLSS	935	-505.5
98	VLSS	990	-505.5
99	VSL	1045	-505.5
100	VSL	1100	-505.5
101	VSS	1155	-505.5
102	NC	1210	-505.5
103	NC	1265	-505.5
104	IREF	1320	-505.5
105	VCOMH	1375	-505.5
106	VCOMH	1430	-505.5
107	VCOMH	1485	-505.5
108	VCOMH	1540	-505.5
109	VCC	1595	-505.5
110	VCC	1650	-505.5
111	VCC	1705	-505.5
112	VCC	1760	-505.5
113	VCC	1815	-505.5
114	NC	1870	-505.5
115	VSS	1925	-505.5
116	TR0	1955	-505.5
117	TR1	1985	-505.5
118	TR2	2015	-505.5
119	VSS	2045	-505.5
120	TR3	2075	-505.5
121	TR4	2105	-505.5
122	TR5	2135	-505.5
123	VSS	2165	-505.5
124	TR6	2195	-505.5
125	TR7	2225	-505.5
126	TR8	2255	-505.5
127	VSS	2285	-505.5
128	TR9	2315	-505.5
129	TR10	2345	-505.5
130	TR11	2375	-505.5
131	VSS	2405	-505.5
132	TR12	2435	-505.5
133	TR13	2465	-505.5
134	TR14	2495	-505.5
135	VSS	2525	-505.5
136	TR15	2555	-505.5
137	TR16	2585	-505.5
138	TR17	2615	-505.5
139	VSS	2645	-505.5
140	TR18	2675	-505.5
141	TR19	2705	-505.5
142	VSS	2735	-505.5
143	NC	2790	-505.5
144	NC	2845	-505.5
145	NC	2900	-505.5
146	NC	2955	-505.5
147	NC	3010	-505.5
148	NC	3065	-505.5
149	NC	3120	-505.5
150	NC	3175	-505.5
151	NC	3230	-505.5
152	NC	3285	-505.5
153	NC	3340	-505.5
154	NC	3395	-505.5
155	NC	3450	-505.5
156	NC	3505	-505.5
157	NC	3560	-505.5
158	NC	3615	-505.5
159	NC	3670	-505.5
160	NC	3725	-505.5
161	NC	3780	-505.5
162	NC	3835	-505.5
163	NC	3890	-505.5
164	NC	3945	-505.5
165	NC	4000	-505.5
166	NC	4055	-505.5
167	NC	4110	-505.5
168	NC	4165	-505.5
169	DR2	4220	-505.5
170	DR3	4275	-505.5
171	NC	4330	-505.5
172	NC	4234.5	501.9
173	DR3	4179.5	501.9
174	DR2	4124.5	501.9
175	SHC	4069.5	480.4
176	RXT3	4040.5	480.4
177	RXT2	4011.5	480.4
178	SHD	3982.5	480.4
179	V33	3808.5	480.4
180	SHE	3779.5	480.4
181	SHF	3750.5	480.4
182	SEG63	3721.5	480.4
183	SEG62	3692.5	480.4
184	SEG61	3663.5	480.4
185	SEG60	3634.5	480.4
186	SEG59	3605.5	480.4
187	SEG58	3576.5	480.4
188	SEG57	3547.5	480.4
189	SEG56	3518.5	480.4
190	SEG55	3489.5	480.4
191	SEG54	3460.5	480.4
192	SEG53	3431.5	480.4
193	SEG52	3402.5	480.4
194	SEG51	3373.5	480.4
195	SEG50	3344.5	480.4
196	SEG49	3315.5	480.4
197	SEG48	3286.5	480.4
198	SEG47	3257.5	480.4
199	SEG46	3228.5	480.4
200	SEG45	3199.5	480.4
201	SEG44	3170.5	480.4
202	SEG43	3141.5	480.4
203	SEG42	3112.5	480.4
204	SEG41	3083.5	480.4
205	SEG40	3054.5	480.4
206	SEG39	3025.5	480.4
207	SEG38	2996.5	480.4
208	SEG37	2967.5	480.4
209	SEG36	2938.5	480.4
210	SEG35	2909.5	480.4
211	SEG34	2880.5	480.4
212	SEG33	2851.5	480.4
213	SEG32	2822.5	480.4
214	SEG31	2793.5	480.4
215	SEG30	2764.5	480.4
216	SEG29	2735.5	480.4
217	SEG28	2706.5	480.4
218	SEG27	2677.5	480.4
219	SEG26	2648.5	480.4
220	SEG25	2619.5	480.4
221	SEG24	2590.5	480.4
222	SEG23	2561.5	480.4
223	SEG22	2532.5	480.4
224	SEG21	2503.5	480.4
225	SEG20	2474.5	480.4
226	SEG19	2445.5	480.4
227	SEG18	2416.5	480.4
228	SEG17	2387.5	480.4
229	SEG16	2358.5	480.4
230	SEG15	2329.5	480.4
231	SEG14	2300.5	480.4
232	SEG13	2271.5	480.4
233	SEG12	2242.5	480.4
234	SEG11	2213.5	480.4
235	SEG10	2184.5	480.4
236	SEG9	2155.5	480.4
237	SEG8	2126.5	480.4
238	SEG7	2097.5	480.4
239	SEG6	2068.5	480.4
240	SEG5	2039.5	480.4

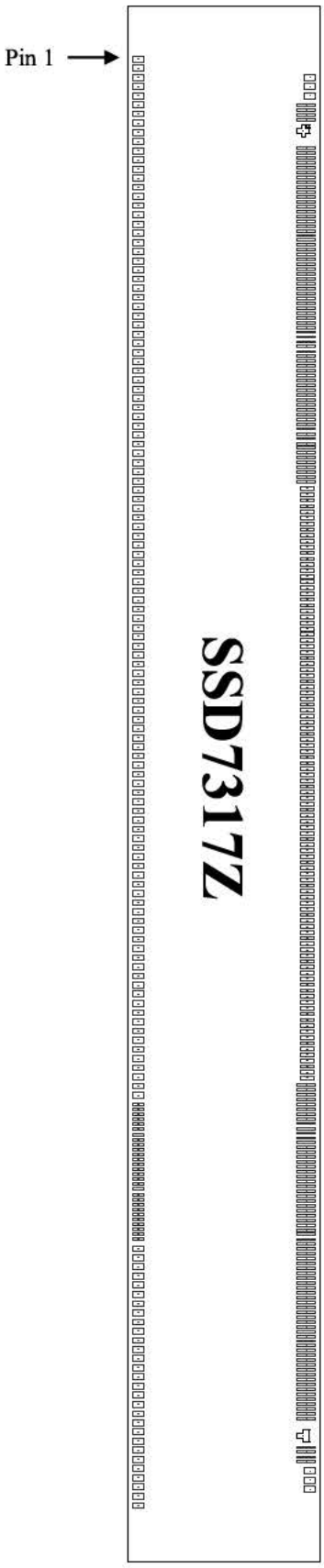
Pin no.	Pin name	x	y
241	SEG4	2010.5	480.4
242	SEG3	1981.5	480.4
243	SEG2	1952.5	480.4
244	SEG1	1923.5	480.4
245	SEG0	1894.5	480.4
246	SHG	1865.5	480.4
247	SHH	1836.5	480.4
248	V33	1807.5	480.4
249	V38	1767.5	484.5
250	V38	1732.5	484.5
251	V38	1697.5	484.5
252	COM0	1662.5	484.5
253	COM1	1627.5	484.5
254	COM2	1592.5	484.5
255	COM3	1557.5	484.5
256	COM4	1522.5	484.5
257	COM5	1487.5	484.5
258	COM6	1452.5	484.5
259	COM7	1417.5	484.5
260	COM8	1382.5	484.5
261	COM9	1347.5	484.5
262	COM10	1312.5	484.5
263	COM11	1277.5	484.5
264	COM12	1242.5	484.5
265	COM13	1207.5	484.5
266	COM14	1172.5	484.5
267	COM15	1137.5	484.5
268	COM16	1102.5	484.5
269	COM17	1067.5	484.5
270	COM18	1032.5	484.5
271	COM19	997.5	484.5
272	COM20	962.5	484.5
273	COM21	927.5	484.5
274	COM22	892.5	484.5
275	COM23	857.5	484.5
276	COM24	822.5	484.5
277	COM25	787.5	484.5
278	COM26	752.5	484.5
279	COM27	717.5	484.5
280	COM28	682.5	484.5
281	COM29	647.5	484.5
282	COM30	612.5	484.5
283	COM31	577.5	484.5
284	COM32	542.5	484.5
285	COM33	507.5	484.5
286	COM34	472.5	484.5
287	COM35	437.5	484.5
288	COM36	402.5	484.5
289	COM37	367.5	484.5
290	COM38	332.5	484.5
291	COM39	297.5	484.5
292	COM40	262.5	484.5
293	COM41	227.5	484.5
294	COM42	192.5	484.5
295	COM43	157.5	484.5
296	COM44	122.5	484.5
297	COM45	87.5	484.5
298	COM46	52.5	484.5
299	COM47	17.5	484.5
300	COM48	-17.5	484.5
301	COM49	-52.5	484.5
302	COM50	-87.5	484.5
303	COM51	-122.5	484.5
304	COM52	-157.5	484.5
305	COM53	-192.5	484.5
306	COM54	-227.5	484.5
307	COM55	-262.5	484.5
308	COM56	-297.5	484.5
309	COM57	-332.5	484.5
310	COM58	-367.5	484.5
311	COM59	-402.5	484.5
312	COM60	-437.5	484.5
313	COM61	-472.5	484.5
314	COM62	-507.5	484.5
315	COM63	-542.5	484.5
316	COM64	-577.5	484.5
317	COM65	-612.5	484.5
318	COM66	-647.5	484.5
319	COM67	-682.5	484.5
320	COM68	-717.5	484.5

Pin no.	Pin name	x	y
321	COM69	-752.5	484.5
322	COM70	-787.5	484.5
323	COM71	-822.5	484.5
324	COM72	-857.5	484.5
325	COM73	-892.5	484.5
326	COM74	-927.5	484.5
327	COM75	-962.5	484.5
328	COM76	-997.5	484.5
329	COM77	-1032.5	484.5
330	COM78	-1067.5	484.5
331	COM79	-1102.5	484.5
332	COM80	-1137.5	484.5
333	COM81	-1172.5	484.5
334	COM82	-1207.5	484.5
335	COM83	-1242.5	484.5
336	COM84	-1277.5	484.5
337	COM85	-1312.5	484.5
338	COM86	-1347.5	484.5
339	COM87	-1382.5	484.5
340	COM88	-1417.5	484.5
341	COM89	-1452.5	484.5
342	COM90	-1487.5	484.5
343	COM91	-1522.5	484.5
344	COM92	-1557.5	484.5
345	COM93	-1592.5	484.5
346	COM94	-1627.5	484.5
347	COM95	-1662.5	484.5
348	V38	-1697.5	484.5
349	V38	-1732.5	484.5
350	V38	-1767.5	484.5
351	V33	-1807.5	480.4
352	SHI	-1836.5	480.4
353	SHJ	-1865.5	480.4
354	SEG64	-1894.5	480.4
355	SEG65	-1923.5	480.4
356	SEG66	-1952.5	480.4
357	SEG67	-1981.5	480.4
358	SEG68	-2010.5	480.4
359	SEG69	-2039.5	480.4
360	SEG70	-2068.5	480.4
361	SEG71	-2097.5	480.4
362	SEG72	-2126.5	480.4
363	SEG73	-2155.5	480.4
364	SEG74	-2184.5	480.4
365	SEG75	-2213.5	480.4
366	SEG76	-2242.5	480.4
367	SEG77	-2271.5	480.4
368	SEG78	-2300.5	480.4
369	SEG79	-2329.5	480.4
370	SEG80	-2358.5	480.4
371	SEG81	-2387.5	480.4
372	SEG82	-2416.5	480.4
373	SEG83	-2445.5	480.4
374	SEG84	-2474.5	480.4
375	SEG85	-2503.5	480.4
376	SEG86	-2532.5	480.4
377	SEG87	-2561.5	480.4
378	SEG88	-2590.5	480.4
379	SEG89	-2619.5	480.4
380	SEG90	-2648.5	480.4
381	SEG91	-2677.5	480.4
382	SEG92	-2706.5	480.4
383	SEG93	-2735.5	480.4
384	SEG94	-2764.5	480.4
385	SEG95	-2793.5	480.4
386	SEG96	-2822.5	480.4
387	SEG97	-2851.5	480.4
388	SEG98	-2880.5	480.4
389	SEG99	-2909.5	480.4
390	SEG100	-2938.5	480.4
391	SEG101	-2967.5	480.4
392	SEG102	-2996.5	480.4
393	SEG103	-3025.5	480.4
394	SEG104	-3054.5	480.4
395	SEG105	-3083.5	480.4
396	SEG106	-3112.5	480.4
397	SEG107	-3141.5	480.4
398	SEG108	-3170.5	480.4
399	SEG109	-3199.5	480.4
400	SEG110	-3228.5	480.4

Pin no.	Pin name	x	y
401	SEG111	-3257.5	480.4
402	SEG112	-3286.5	480.4
403	SEG113	-3315.5	480.4
404	SEG114	-3344.5	480.4
405	SEG115	-3373.5	480.4
406	SEG116	-3402.5	480.4
407	SEG117	-3431.5	480.4
408	SEG118	-3460.5	480.4
409	SEG119	-3489.5	480.4
410	SEG120	-3518.5	480.4
411	SEG121	-3547.5	480.4
412	SEG122	-3576.5	480.4
413	SEG123	-3605.5	480.4
414	SEG124	-3634.5	480.4
415	SEG125	-3663.5	480.4
416	SEG126	-3692.5	480.4
417	SEG127	-3721.5	480.4
418	SHK	-3750.5	480.4
419	SHL	-3779.5	480.4
420	V33	-3808.5	480.4
421	SHM	-3982.5	480.4
422	RXT1	-4011.5	480.4
423	RXT0	-4040.5	480.4
424	SHN	-4069.5	480.4
425	DR1	-4124.5	501.9
426	DR0	-4179.5	501.9
427	NC	-4234.5	501.9

Appendix II: SSD7317Z Die Pad oor Plan

Figure 1-1: – SSD7317Z Die drawing

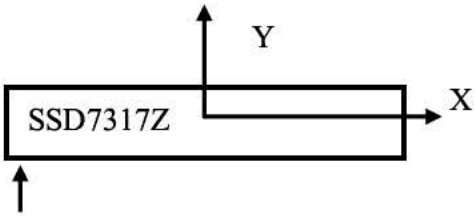


Die size	9.33 mm +/- 0.05mm x 1.13 mm+/- 0.05mm
Die thickness	250 +/- 15um
Min I/O pad pitch	30um
Min SEG pad pitch	29um
Min COM pad pitch	35um
Bump height	Nominal 9 um

Bump size		
Pad#	X[um]	Y[um]
1-114, 143-174, 425-427	35	67
115-142	15	67
175-248, 351-424	14	110
249-350	20	80

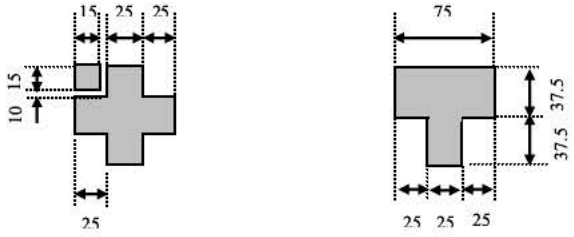
Alignment mark	Position	Size
+ shape	(-3913.5, 462.4)	75um x 75um
T shape	(3913.5, 462.4)	75um x 75um
SSL Logo	(4470.4, 146.5)	-

(For details dimension please see **Figure 1-2**)



Pad 1,2,3,…->171
Gold Bumps face up

Figure 1-2: SSD7317Z alignment mark dimension



Center: (-3913.5, 462.4)
Size: 75 x 75 μm²

Center: (3913.5, 462.4)
Size: 75 x 75 μm²

Appendix III: SSD7317 Command Table and Command Descriptions

1) COMMAND TABLE

Table 0-2: SSD7317 Command Table

(D/C#=0, R/W#(WR#) = 0, E(RD#=1) unless specific setting is stated)

<table>
<tr><th colspan="11">Fundamental Command Table</th></tr>
<tr><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>00~0F</td><td>0</td><td>0</td><td>0</td><td>0</td><td>X_3</td><td>X_2</td><td>X_1</td><td>X_0</td><td>Set Lower Column Start Address for Page Addressing Mode</td><td>Set the lower nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET.

Note
(1) This command is only for page addressing mode</td></tr>
<tr><td>0</td><td>10~17</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>X_2</td><td>X_1</td><td>X_0</td><td>Set Higher Column Start Address for Page Addressing Mode</td><td>Set the higher nibble of the column start address register for Page Addressing Mode using X[2:0] as data bits. The initial display line register is reset to 0000b after RESET.

Note
(1) This command is only for page addressing mode</td></tr>
<tr><td>0
0</td><td>20
A[3]
A[1:0]</td><td>0
*</td><td>0
*</td><td>1
*</td><td>0
*</td><td>0
A_3</td><td>0
*</td><td>0
A_1</td><td>0
A_0</td><td>Set Memory Addressing Mode</td><td>
<table>
<tr><th>A[3]</th><th>A[1:0]</th><th>Addressing Modes</th></tr>
<tr><td>0b</td><td>01b</td><td>COM-Page H-Mode</td></tr>
<tr><td>0b</td><td>10b</td><td>Page Addressing Mode (RESET)</td></tr>
<tr><td>1b</td><td>01b</td><td>SEG-Page H-Mode</td></tr>
</table>
Note
(1) Setting other than the above table is invalid.</td></tr>
<tr><td>0
0
0</td><td>21
A[6:0]
B[6:0]</td><td>0
0
0</td><td>0
A_6
B_6</td><td>1
A_5
B_5</td><td>0
A_4
B_4</td><td>0
A_3
B_3</td><td>0
A_2
B_2</td><td>0
A_1
B_1</td><td>1
A_0
B_0</td><td>Set Line Address</td><td>Setup line start and end address

In COM-Page H-mode,
A[6:0] : Set Row start address,
range : 0-127d, (RESET=0d)
B[6:0]: Set Row end address,
range : 0-127d, (RESET =127d)

In SEG-Page H-mode,
A[6:0] : Set Column start address,
range : 0-95d, (RESET=0d)
B[6:0]: Set Column end address,
range : 0-95d, (RESET=95d)

Note
(1) This command is only for COM-Page H-mode and SEG-Page H-mode.
(2) Column defines the graphic display data RAM column (along COM direction) while Row defines the Graphic display data RAM row (along SEG direction).</td></tr>
</table>

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 0 0	22 A[3:0] B[3:0]	0 * *	0 * *	1 * *	0 * *	0 A_3 B_3	0 A_2 B_2	1 A_1 B_1	0 A_0 B_0	Set Page Address	Setup page start and end address In COM-Page H-mode, A[6:0] : Set COM-Page start Address, range 0-11d, (RESET = 0d) B[6:0]: Set COM-Page end address, range : 0-11d, (RESET = 11d) In SEG-Page H-mode, A[6:0] : Set SEG-Page start Address, range 0-15d, (RESET = 0d) B[6:0]: Set SEG-Page end address, range : 0-15d, (RESET = 15d) **Note** (1) This command is only for COM-Page H-mode and SEG-Page H-mode. (2) The Page in SEG-Page is a transpose of the Page in COM-Page mode. Page in COM-Page mode defines a group of 8-bit COM data on the same SEG line, while Page in SEG-Page mode defines a group of 8-bit SEG data in the same COM line.
0	40~7F	0	1	X_5	X_4	X_3	X_2	X_1	X_0	Set Display Start Line	Set display RAM display start line register from 0-63 using $X_5X_4X_3X_2X_1X_0$. Display start line register is reset to 000000b during RESET. **Note** (1) For display start line register up to 95, please refer to command A2h.
0 0	81 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Contrast Control	Double byte command to select one of the contrast steps. Contrast increases as the value increases. (RESET = 7Fh) A[7:0] valid range: 01h to FFh
0	A0/A1	1	0	1	0	0	0	0	X_0	Set Segment Re-map	A0h, X[0]=0b: column address 0 is mapped to SEG0 (RESET) A1h, X[0]=1b: column address 127 is mapped to SEG0
0 0	A2 A[6:0]	1 0	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Display Start Line	Set display RAM display start line register from 0-95 by A[6:0] (RESET=00h) **Note** (1) In command A2h, A[6:0] from 00h to 3Fh has the same effect as command 40h-7Fh.
0	A4/A5	1	0	1	0	0	1	0	X_0	Entire Display ON	A4h, X_0=0b: Resume to RAM content display (RESET) Output follows RAM content A5h, X_0=1b: Entire display ON Output ignores RAM content

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	A6/A7	1	0	1	0	0	1	1	X_0	Set Normal/Inverse Display	A6h, X[0]=0b: Normal display (RESET) 0 in RAM: OFF in display panel 1 in RAM: ON in display panel A7h, X[0]=1b: Inverse display 0 in RAM: ON in display panel 1 in RAM: OFF in display panel
0 0	A8 A[6:0]	1 *	0 A_6	1 A_5	0 A_4	1 A_3	0 A_2	0 A_1	0 A_0	Set Multiplex Ratio	Set MUX ratio to N+1 MUX N=A[6:0] : from 16MUX to 96MUX. RESET= 101 1111b (i.e. 95d, 96MUX) A[6:0] from 0 to 14 are invalid entry.
0 0	AD A[4]	1 0	0 0	1 0	0 A_4	1 0	1 0	0 0	1 0	External or internal I_{REF} Selection	Select external or internal I_{REF} : A[4] = '0' Select external I_{REF} (RESET) A[4] = '1' Enable internal I_{REF} during display ON **Note** (1) Refer to section 6.8 in SSD7317 datasheet for details.
0	AE/AF	1	0	1	0	1	1	1	X_0	Set Display ON/OFF	AEh, X[0]=0b: Display OFF (sleep mode) (RESET) AFh X[0]=1b: Display ON in normal mode
0	B0~BB	1	0	1	1	X_3	X_2	X_1	X_0	Set Page Start Address for Page Addressing Mode	Set GDDRAM Page Start Address (PAGE0~PAGE11) for Page Addressing Mode using X[3:0]. **Note** (1) This command is only for page addressing mode
0	C0/C8	1	1	0	0	X_3	0	0	0	Set COM Output Scan Direction	C0h, X[3]=0b: normal mode (RESET) Scan from COM0 to COM[N –1] C8h, X[3]=1b: remapped mode. Scan from COM[N-1] to COM0 Where N is the Multiplex ratio.
0 0	D3 A[6:0]	1 *	1 A_6	0 A_5	1 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Set Display Offset	Set line shift by COM from 0d~95d The value is reset to 00h after RESET.
0 0	D5 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	0 A_3	1 A_2	0 A_1	1 A_0	t Display lock Divide atio/Oscillator requency	A[3:0]: Define divide ratio (D) of display clock (DCLK) (i.e. 1, 2, 3, …, 16) (RESET is 0000b, i.e. divide ratio = 1) A[7:4] : Set the Oscillator Frequency, F_{OSC}. Oscillator Frequency increases with the value of A[7:4] and vice versa. (RESET is 1011b) Range: 0000b~1111b.

<table>
<tr><th colspan="11">Fundamental Command Table</th></tr>
<tr><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0
0</td><td>D9
A[7:0]</td><td>1
A_7</td><td>1
A_6</td><td>0
A_5</td><td>1
A_4</td><td>1
A_3</td><td>0
A_2</td><td>0
A_1</td><td>1
A_0</td><td>Set Pre-charge Period</td><td>A[3:0] : Phase 1 period of up to 30 DCLK (ie. 2, 4, 6, …, 30)
Clock 0 is invalid entry
(RESET=2h)

A[7:4] : Phase 2 period of up to 30 DCLK (ie. 2, 4, 6, …, 30)
Clock 0 is invalid entry
(RESET=2h)</td></tr>
<tr><td>0
0</td><td>DA
A[5:4]</td><td>1
0</td><td>1
0</td><td>0
A_5</td><td>1
A_4</td><td>1
0</td><td>0
0</td><td>1
1</td><td>0
0</td><td>Set SEG Pins Hardware Configuration</td><td>A[4]=0b, Sequential SEG pin configuration
A[4]=1b (RESET), Alternative (odd/even) SEG pin configuration

A[5]=0b (RESET), Disable SEG Left/Right remap
A[5]=1b, Enable SEG Left/Right remap</td></tr>
<tr><td>0
0</td><td>DB
A[5:3]</td><td>1
0</td><td>1
0</td><td>0
A_5</td><td>1
A_4</td><td>1
A_3</td><td>0
0</td><td>1
0</td><td>1
0</td><td>Set V_{COMH} select Level</td><td>Set COM select voltage level.
<table><tr><th>A[5:3]</th><th>Hex code</th><th>V_{COMH} deselect level</th></tr><tr><td>100b</td><td>20h</td><td>~ 0.67 x V_{CC}</td></tr><tr><td>110b</td><td>30h</td><td>~ 0.78 x V_{CC} (RESET)</td></tr><tr><td>111b</td><td>38h</td><td>~ 0.84 x V_{CC}</td></tr></table></td></tr>
<tr><td>0</td><td>E3</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>NOP</td><td>Command for no operation</td></tr>
<tr><td>0
0</td><td>FD
A[2]</td><td>1
0</td><td>1
0</td><td>1
0</td><td>1
1</td><td>1
0</td><td>1
A_2</td><td>0
1</td><td>1
0</td><td>Set Command Lock</td><td>A[2]: MCU protection status.

A[2] = 0b, Unlock OLED driver IC MCU interface from entering command (RESET)
A[2] = 1b, Lock OLED driver IC MCU interface from entering command

Note
(1) The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command</td></tr>
</table>

Note
(1) "*" stands for "Don't care".

Table 0-3 : Read Command Table

Bit Pattern	Command	Description
$D_7D_6D_5D_4D_3D_2D_1D_0$	Status Register Read	D[7] : Reserved D[6] : "1" for display OFF / "0" for display ON D[5] : Reserved D[4] : Reserved D[3] : Reserved D[2] : Reserved D[1] : Reserved D[0] : Reserved

Note
(1) Patterns other than those given in the Command Table are prohibited to enter the chip as a command; as unexpected results can occur.

a. Data Read / Write

To read data from the GDDRAM, select HIGH for both the R/W# (WR#) pin and the D/C# pin for 6800-series parallel mode and select LOW for the E (RD#) pin and HIGH for the D/C# pin for 8080-series parallel mode. No data read is provided in serial mode operation.
In normal data read mode the GDDRAM column address pointer will be increased automatically by one after each data read.
Also, a dummy read is required before the first data read.
To write data to the GDDRAM, select LOW for the R/W# (WR#) pin and HIGH for the D/C# pin for both 6800-series parallel mode and 8080-series parallel mode. The serial interface mode is always in write mode. The GDDRAM column address pointer will be increased automatically by one after each data write.

Table 0-4 : Address increment table (Automatic)

D/C#	R/W# (WR#)	Comment	Address Increment
0	0	Write Command	No
0	1	Read Status	No
1	0	Write Data	Yes
1	1	Read Data	Yes

2) COMMAND DESCRIPTIONS

a. Fundamental Command

i. Set Lower Column Start Address for Page Addressing Mode (00h~0Fh)

This command specifies the lower nibble of the 8-bit column start address for the display data RAM under Page Addressing Mode. The column address will be incremented by each data access. Please refer to Table 0-2 and Section iii for details.

ii. Set Higher Column Start Address for Page Addressing Mode (10h~17h)

This command specifies the higher nibble of the 8-bit column start address for the display data RAM under Page Addressing Mode. The column address will be incremented by each data access. Please refer to Table 0-2 and Section iii for details.

iii. Set Memory Addressing Mode (20h)

There are different memory addressing modes in SSD7317: page addressing mode, COM-Page H-mode and SEG-Page H-mode. User can sets the way of memory addressing by command 20h.

Page addressing mode (A[3:0]=0010b)

In page addressing mode, after the display RAM is read / written, the column address pointer is increased automatically by 1 and page address pointer is not changed. Users have to set the new page and column addresses in order to access the next page RAM content. The sequence of movement of the PAGE and column address point for page addressing mode is shown in Figure 0-3.

Figure 0-3 : Address Pointer Movement of Page addressing mode

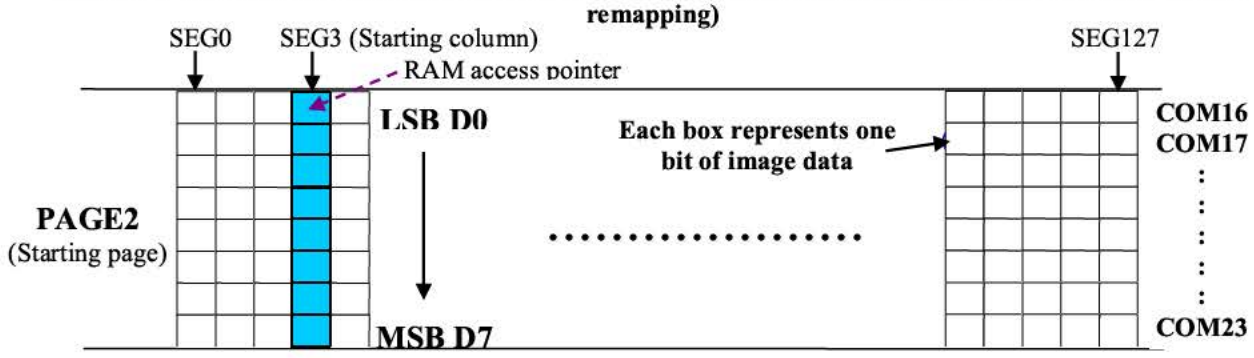
	COL0	COL 1	…..	COL 126	COL 127
PAGE0	→	→	→	→	→
PAGE1	→	→	→	→	→
:	→	→	→	→	→
PAGE10	→	→	→	→	→
PAGE11	→	→	→	→	→

In normal display data RAM read or write and page addressing mode, the following steps are required to define the starting RAM access pointer location:

- Set the page start address of the target display location by command B0h to BBh.
- Set the lower start column address of pointer by command 00h~0Fh.
- Set the higher start column address of pointer by command 10h~17h.

For example, if the page start address is set to B2h, lower column address is 03h and higher column address is 10h, then that means the starting column is SEG3 of PAGE2. The RAM access pointer is located as shown in Figure 0-5. The input data byte will be written into RAM position of column 3.

Figure 0-4 : Example of GDDRAM access pointer setting in Page Addressing Mode (No row and column-remapping)



COM-Page and SEG-Page

SEG-Page provides a flexibility to transpose the RAM write orientation from COM-Page. Page in COM-Page mode defines a group of 8-bit COM data on the same SEG line, while Page in SEG-Page mode defines a group of 8-bit SEG data in the same COM line. The term "COL" means the graphic display data RAM column (along COM direction) while "ROW" means the graphic display data RAM row (along SEG direction). Figure 0-5 and **Figure 0-6** show the RAM orientation of a Page in COM-Page mode and SEG-Page mode respectively.

Figure 0-5 : GDDRAM access pointer setting and orientation (No row and column-remapping) in COM-Page Mode

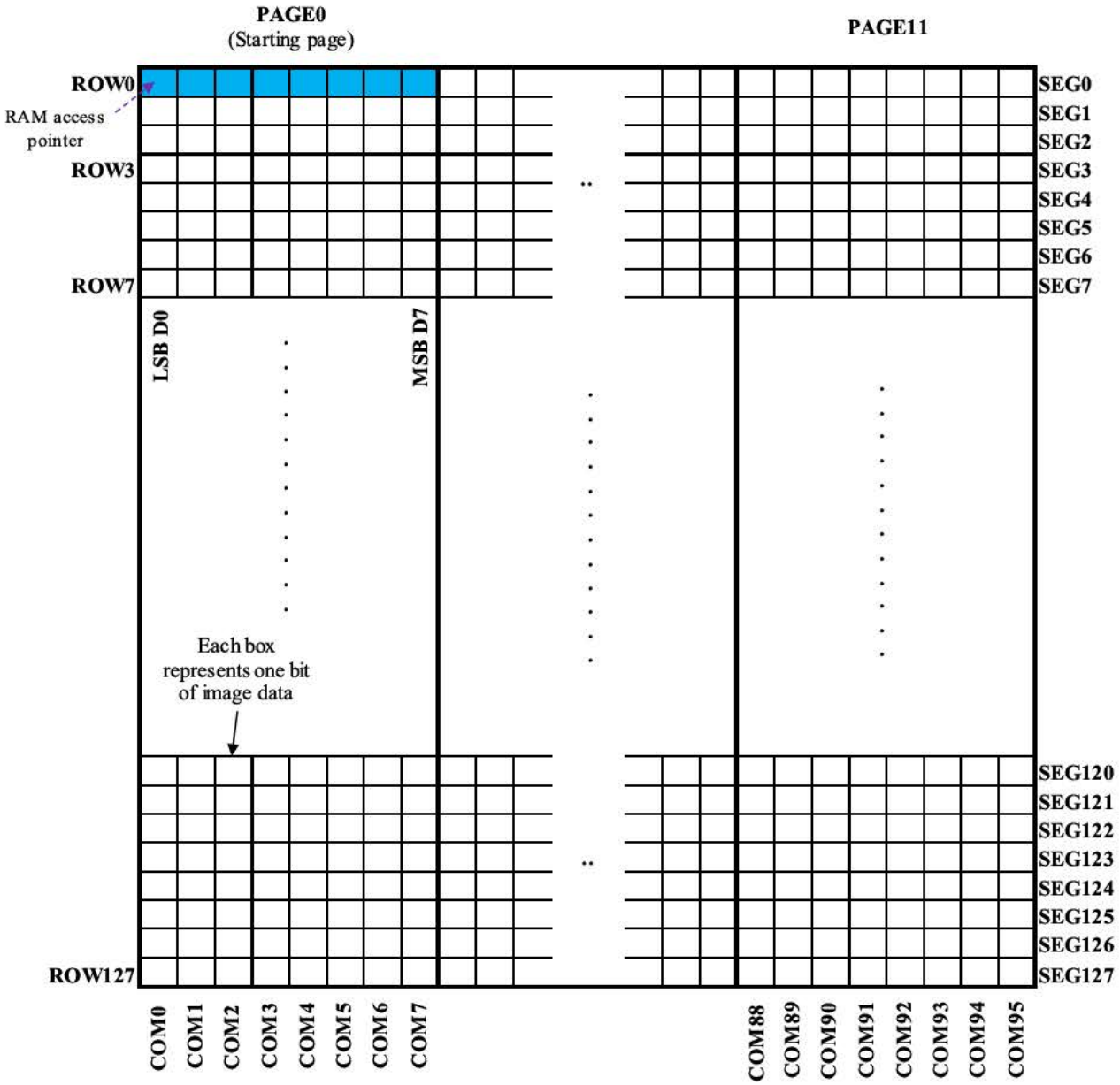
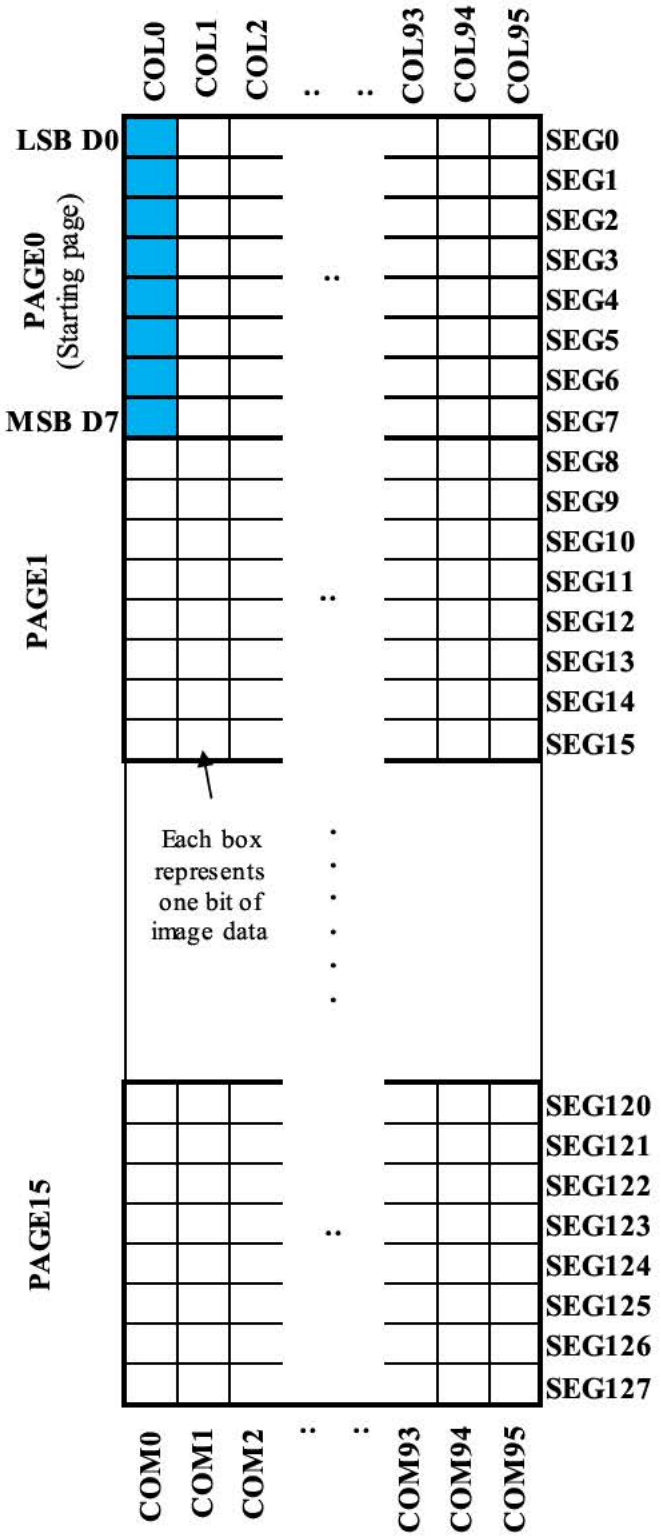


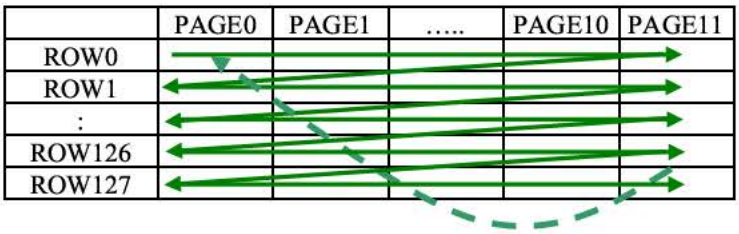
Figure 0-6 : GDDRAM access pointer setting and orientation (No row and column-remapping) in SEG-Page Mode



COM-Page H-mode (A[3:0]=0001b)

In COM-Page H-mode, after the display RAM is read / written, the page (COM-Page) address pointer is increased automatically by 1. If the page address pointer reaches the page end address, the page address pointer is reset to page start address and row (line) address pointer is increased by 1. The sequence of movement of the page and row address point for COM-Page H-mode is shown in Figure 0-7. When both row and page address pointers reach the end address, the pointers are reset to row start address and page start address (Dotted line in Figure 0-7.)

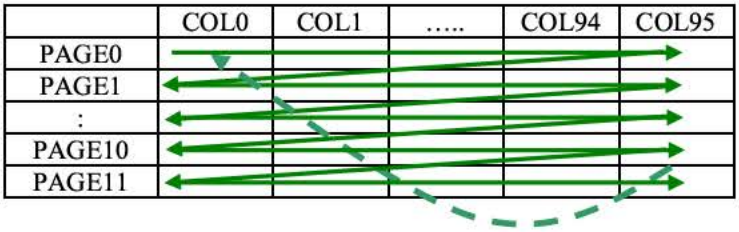
Figure 0-7 : Address Pointer Movement of COM-Page H-mode



SEG-Page H-mode (A[3:0]=1001b)

In SEG-Page H-mode, the column (line) address pointer increased automatically by 1 every time the display RAM is written. The column address pointer reset to column start address and page (SEG-Page) address pointer is increased by 1 if the column address pointer reaches column end address. The column address and page address pointers are reset to column start address and page start address if both column and page address pointers reach the end address. The sequence of movement of the page and column address pointer for SEG-Page H-mode is shown in Figure 0-8.

Figure 0-8 : Address Pointer Movement of SEG-Page H-mode



In normal display data RAM read or write in COM-Page or SEG-Page mode, the following steps are required to define the RAM access pointer location:

- Set the line start and end address of the target display location by command 21h.
- Set the page start and end address of the target display location by command 22h.

Example is shown in Figure 0-9.

iv. Set Line Address (21h)

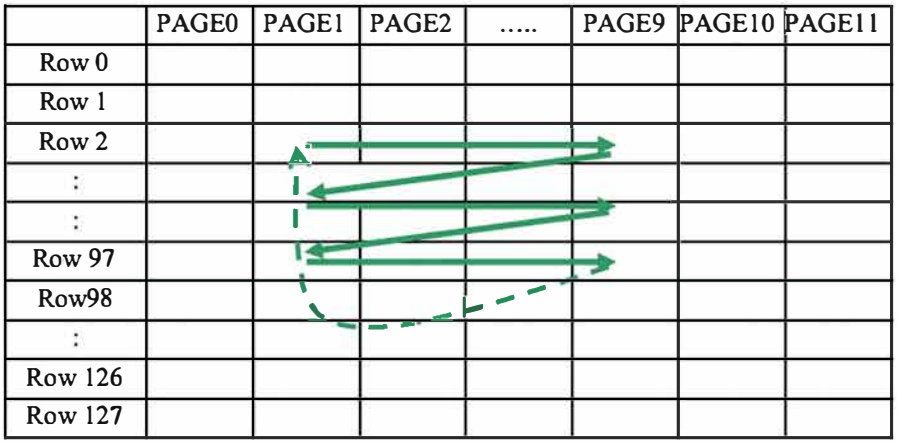
This triple byte command specifies line start address and end address of the display data RAM. This command also sets the row address pointer to row start address in COM-Page mode and sets the column address pointer to column start address in SEG-Page mode. This pointer is used to define the current read/write line address in graphic display data RAM. If COM-Page H mode or SEG-Page H-mode is enabled by command 20h, after finishing read/write one line data (one row in COM-Page H-mode or one column in SEG-Page H-mode), it is incremented automatically to the next line address. Whenever the line address pointer finishes accessing the end line address, it is reset back to start line address and the page address is incremented to the next page.

v. Set Page Address (22h)

This triple byte command specifies page start address and end address of the display data RAM. This command also sets the page address pointer to page start address. This pointer is used to define the current read/write page address in graphic display data RAM. If COM-Page H-mode or SEG-Page H-mode is enabled by command 20h, after finishing read/write one page data, it is incremented automatically to the next page address. Whenever the page address pointer finishes accessing the end page address, it is reset back to start page address.

The figure below shows the way of line (row or column) and page address pointer movement in COM-Page H-mode through the example: page start address is set to 1 and page end address is set to 9, row start address is set to 2 and row end address is set to 97; COM-Page H-mode is enabled by command 20h. In this case, the graphic display data RAM row accessible range is from page 1 to page 9 and from row 2 to row 97 only. In addition, the page address pointer is set to 1 and row address pointer is set to 2. After finishing read/write one pixel of data, the page address is increased automatically by 1 to access the next RAM location for next read/write operation (*solid line in Figure 0-9*). Whenever the page address pointer finishes accessing the end page 9, it is reset back to page 1 and row address is automatically increased by 1 (*solid line in Figure 0-9*). While the end page 9 and end row 97 RAM location is accessed, the page address is reset back to 1 and the row address is reset back to 2 (*dotted line in Figure 0-9*).

Figure 0-9: Example of Address Pointer Movement



vi. Set Display Start Line (40h~7Fh)

This command sets the Display Start Line register to determine starting address of display RAM, by selecting a value from 0 to 63. With value equal to 0, RAM row 0 is mapped to COM0. With value equal to 1, RAM row 1 is mapped to COM0 and so on. Refer to Table 0-5 for more illustrations. For display start line register setting up to 95, please refer to command A2h.

vii. Set Contrast Control (81h)

This command sets the Contrast Setting of the display, with a valid range from 01h to FFh. The segment output current increases as the contrast step value increase.

viii. Set Segment Re-map (A0h/A1h)

This command changes the mapping between the display data column address and the segment driver. It allows flexibility in OLED module design. Please refer to Table 0-2.

This command only affects subsequent data input. Data already stored in GDDRAM will have no changes.

ix. Set Display Start Line (A2h)

This double byte command sets the Display Start Line register to determine starting address of display RAM, by selecting a value from 0 to 95. With value equal to 0, RAM row 0 is mapped to COM0. With value equal to 1, RAM row 1 is mapped to COM0 and so on. Refer to Table 0-5 for more illustrations. The value setting from 0 to 63 has the same effect as single byte command 40h-7Fh.

x. Entire Display ON (A4h/A5h)

A4h command enable display outputs according to the GDDRAM contents.
If A5h command is issued, then by using A4h command, the display will resume to the GDDRAM contents. In other words, A4h command resumes the display from entire display "ON" stage.
A5h command forces the entire display to be "ON", regardless of the contents of the display data RAM.

xi. Set Normal/Inverse Display (A6h/A7h)

This command sets the display to be either normal or inverse. In normal display a RAM data of 1 indicates an "ON" pixel while in inverse display a RAM data of 0 indicates an "ON" pixel.

xii. Set Multiplex Ratio (A8h)

This command switches the default 96 multiplex mode to any multiplex ratio, ranging from 16 to 95. The output pads COM0~COM95 will be switched to the corresponding COM signal.

xiii. External or internal IREF Selection (ADh)

This double byte command supports External or Internal I_{REF} Selection.

Default A[4] = '0', Select external I_{REF}.

When A[4] = '1', Select internal I_{REF} during display ON.

xiv. Set Display ON/OFF (AEh/AFh)

These single byte commands are used to turn the OLED panel display ON or OFF.
When the display is ON, the selected circuits by Set Master Configuration command will be turned ON.
When the display is OFF, those circuits will be turned OFF and the segment and common output are in V_{SS} state and high impedance state, respectively. These commands set the display to one of the two states:

- AEh : Display OFF
- AFh : Display ON

Figure 0-10 : Transition between different modes

xv. Set Page Start Address for Page Addressing Mode (B0h~BBh)

This command positions the page start address from 0 to 11 in GDDRAM under Page Addressing Mode. Please refer to Table 0-2 and Section iii for details.

vi. Set COM Output Scan Direction (C0h/C8h)

This command sets the scan direction of the COM output, allowing layout flexibility in the OLED module design. Additionally, the display will show once this command is issued. For example, if this command is sent during normal display then the graphic display will be vertically flipped immediately. Please refer to Table 0-7 for details.

xvii. Set Display Offset (D3h)

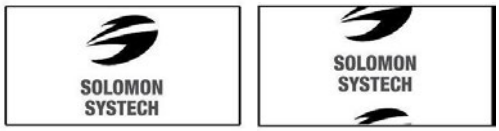
This is a double byte command. The second command specifies the mapping of the display start line to one of COM0~COM95 (assuming that COM0 is the display start line then the display start line register is equal to 0).

For example, to move the COM16 towards the COM0 direction by 16 lines the 7-bit data in the second byte should be given as 0010000b. To move in the opposite direction by 16 lines the 7-bit data should be given by 96 – 16, so the second byte would be 1010000b. The following two tables (Table 0-5 and Table 0-6) show the examples of setting the command C0h/C8h and D3h.

Table 0-5: Example of Set Display Offset and Display Start Line without Remap

	Output												
	96		96		96		80		80		80		Set MUX ratio(A8h)
	Normal		Normal		Normal		Normal		Normal		Normal		COM Normal / R mapp d (C0h / C8h)
Hardware	0		8		0		0		8		0		Display offs t (D3h)
pin name	0		0		8		0		0		8		Display start line (A2h)
COM0	Row0	RAM0	Row8	RAM8	Row0	RAM8	Row0	RAM0	Row8	RAM8	Row0	RAM8	
COM1	Row1	RAM1	Row9	RAM9	Row1	RAM9	Row1	RAM1	Row9	RAM9	Row1	RAM9	
COM2	Row2	RAM2	Row10	RAM10	Row2	RAM10	Row2	RAM2	Row10	RAM10	Row2	RAM10	
COM3	Row3	RAM3	Row11	RAM11	Row3	RAM11	Row3	RAM3	Row11	RAM11	Row3	RAM11	
COM4	Row4	RAM4	Row12	RAM12	Row4	RAM12	Row4	RAM4	Row12	RAM12	Row4	RAM12	
COM5	Row5	RAM5	Row13	RAM13	Row5	RAM13	Row5	RAM5	Row13	RAM13	Row5	RAM13	
COM6	Row6	RAM6	Row14	RAM14	Row6	RAM14	Row6	RAM6	Row14	RAM14	Row6	RAM14	
COM7	Row7	RAM7	Row15	RAM15	Row7	RAM15	Row7	RAM7	Row15	RAM15	Row7	RAM15	
COM8	Row8	RAM8	Row16	RAM16	Row8	RAM16	Row8	RAM8	Row16	RAM16	Row8	RAM16	
COM9	Row9	RAM9	Row17	RAM17	Row9	RAM17	Row9	RAM9	Row17	RAM17	Row9	RAM17	
COM10	Row10	RAM10	Row18	RAM18	Row10	RAM18	Row10	RAM10	Row18	RAM18	Row10	RAM18	
COM11	Row11	RAM11	Row19	RAM19	Row11	RAM19	Row11	RAM11	Row19	RAM19	Row11	RAM19	
COM12	Row12	RAM12	Row20	RAM20	Row12	RAM20	Row12	RAM12	Row20	RAM20	Row12	RAM20	
COM13	Row13	RAM13	Row21	RAM21	Row13	RAM21	Row13	RAM13	Row21	RAM21	Row13	RAM21	
COM14	Row14	RAM14	Row22	RAM22	Row14	RAM22	Row14	RAM14	Row22	RAM22	Row14	RAM22	
COM15	Row15	RAM15	Row23	RAM23	Row15	RAM23	Row15	RAM15	Row23	RAM23	Row15	RAM23	
COM16	Row16	RAM16	Row24	RAM24	Row16	RAM24	Row16	RAM16	Row24	RAM24	Row16	RAM24	
COM17	Row17	RAM17	Row25	RAM25	Row17	RAM25	Row17	RAM17	Row25	RAM25	Row17	RAM25	
COM18	Row18	RAM18	Row26	RAM26	Row18	RAM26	Row18	RAM18	Row26	RAM26	Row18	RAM26	
COM19	Row19	RAM19	Row27	RAM27	Row19	RAM27	Row19	RAM19	Row27	RAM27	Row19	RAM27	
COM20	Row20	RAM20	Row28	RAM28	Row20	RAM28	Row20	RAM20	Row28	RAM28	Row20	RAM28	
COM21	Row21	RAM21	Row29	RAM29	Row21	RAM29	Row21	RAM21	Row29	RAM29	Row21	RAM29	
COM22	Row22	RAM22	Row30	RAM30	Row22	RAM30	Row22	RAM22	Row30	RAM30	Row22	RAM30	
COM23	Row23	RAM23	Row31	RAM31	Row23	RAM31	Row23	RAM23	Row31	RAM31	Row23	RAM31	
COM24	Row24	RAM24	Row32	RAM32	Row24	RAM32	Row24	RAM24	Row32	RAM32	Row24	RAM32	
COM25	Row25	RAM25	Row33	RAM33	Row25	RAM33	Row25	RAM25	Row33	RAM33	Row25	RAM33	
COM26	Row26	RAM26	Row34	RAM34	Row26	RAM34	Row26	RAM26	Row34	RAM34	Row26	RAM34	
COM27	Row27	RAM27	Row35	RAM35	Row27	RAM35	Row27	RAM27	Row35	RAM35	Row27	RAM35	
COM28	Row28	RAM28	Row36	RAM36	Row28	RAM36	Row28	RAM28	Row36	RAM36	Row28	RAM36	
COM29	Row29	RAM29	Row37	RAM37	Row29	RAM37	Row29	RAM29	Row37	RAM37	Row29	RAM37	
COM30	Row30	RAM30	Row38	RAM38	Row30	RAM38	Row30	RAM30	Row38	RAM38	Row30	RAM38	
COM31	Row31	RAM31	Row39	RAM39	Row31	RAM39	Row31	RAM31	Row39	RAM39	Row31	RAM39	
COM32	Row32	RAM32	Row40	RAM40	Row32	RAM40	Row32	RAM32	Row40	RAM40	Row32	RAM40	
COM33	Row33	RAM33	Row41	RAM41	Row33	RAM41	Row33	RAM33	Row41	RAM41	Row33	RAM41	
COM34	Row34	RAM34	Row42	RAM42	Row34	RAM42	Row34	RAM34	Row42	RAM42	Row34	RAM42	
COM35	Row35	RAM35	Row43	RAM43	Row35	RAM43	Row35	RAM35	Row43	RAM43	Row35	RAM43	
COM36	Row36	RAM36	Row44	RAM44	Row36	RAM44	Row36	RAM36	Row44	RAM44	Row36	RAM44	
COM37	Row37	RAM37	Row45	RAM45	Row37	RAM45	Row37	RAM37	Row45	RAM45	Row37	RAM45	
COM38	Row38	RAM38	Row46	RAM46	Row38	RAM46	Row38	RAM38	Row46	RAM46	Row38	RAM46	
COM39	Row39	RAM39	Row47	RAM47	Row39	RAM47	Row39	RAM39	Row47	RAM47	Row39	RAM47	
COM40	Row40	RAM40	Row48	RAM48	Row40	RAM48	Row40	RAM40	Row48	RAM48	Row40	RAM48	
COM41	Row41	RAM41	Row49	RAM49	Row41	RAM49	Row41	RAM41	Row49	RAM49	Row41	RAM49	
COM42	Row42	RAM42	Row50	RAM50	Row42	RAM50	Row42	RAM42	Row50	RAM50	Row42	RAM50	
COM43	Row43	RAM43	Row51	RAM51	Row43	RAM51	Row43	RAM43	Row51	RAM51	Row43	RAM51	
COM44	Row44	RAM44	Row52	RAM52	Row44	RAM52	Row44	RAM44	Row52	RAM52	Row44	RAM52	
COM45	Row45	RAM45	Row53	RAM53	Row45	RAM53	Row45	RAM45	Row53	RAM53	Row45	RAM53	
COM46	Row46	RAM46	Row54	RAM54	Row46	RAM54	Row46	RAM46	Row54	RAM54	Row46	RAM54	
COM47	Row47	RAM47	Row55	RAM55	Row47	RAM55	Row47	RAM47	Row55	RAM55	Row47	RAM55	
COM48	Row48	RAM48	Row56	RAM56	Row48	RAM56	Row48	RAM48	Row56	RAM56	Row48	RAM56	
COM49	Row49	RAM49	Row57	RAM57	Row49	RAM57	Row49	RAM49	Row57	RAM57	Row49	RAM57	
COM50	Row50	RAM50	Row58	RAM58	Row50	RAM58	Row50	RAM50	Row58	RAM58	Row50	RAM58	
COM51	Row51	RAM51	Row59	RAM59	Row51	RAM59	Row51	RAM51	Row59	RAM59	Row51	RAM59	
COM52	Row52	RAM52	Row60	RAM60	Row52	RAM60	Row52	RAM52	Row60	RAM60	Row52	RAM60	
COM53	Row53	RAM53	Row61	RAM61	Row53	RAM61	Row53	RAM53	Row61	RAM61	Row53	RAM61	
COM54	Row54	RAM54	Row62	RAM62	Row54	RAM62	Row54	RAM54	Row62	RAM62	Row54	RAM62	
COM55	Row55	RAM55	Row63	RAM63	Row55	RAM63	Row55	RAM55	Row63	RAM63	Row55	RAM63	
COM56	Row56	RAM56	Row64	RAM64	Row56	RAM64	Row56	RAM56	Row64	RAM64	Row56	RAM64	
COM57	Row57	RAM57	Row65	RAM65	Row57	RAM65	Row57	RAM57	Row65	RAM65	Row57	RAM65	
COM58	Row58	RAM58	Row66	RAM66	Row58	RAM66	Row58	RAM58	Row66	RAM66	Row58	RAM66	
COM59	Row59	RAM59	Row67	RAM67	Row59	RAM67	Row59	RAM59	Row67	RAM67	Row59	RAM67	
COM60	Row60	RAM60	Row68	RAM68	Row60	RAM68	Row60	RAM60	Row68	RAM68	Row60	RAM68	
COM61	Row61	RAM61	Row69	RAM69	Row61	RAM69	Row61	RAM61	Row69	RAM69	Row61	RAM69	
COM62	Row62	RAM62	Row70	RAM70	Row62	RAM70	Row62	RAM62	Row70	RAM70	Row62	RAM70	
COM63	Row63	RAM63	Row71	RAM71	Row63	RAM71	Row63	RAM63	Row71	RAM71	Row63	RAM71	

	Output												
	96		96		96		80		80		80		Set MUX ratio(A8h)
	Normal		Normal		Normal		Normal		Normal		Normal		COM Normal / Remapped (C0h / C8h)
Hardware	0		8		0		0		8		0		Display offset (D3h)
pin name	0		0		8		0		0		8		Display start line (A2h)
COM64	Row64	RAM64	Row72	RAM72	Row64	RAM72	Row64	RAM64	Row72	RAM72	Row64	RAM72	
COM65	Row65	RAM65	Row73	RAM73	Row65	RAM73	Row65	RAM65	Row73	RAM73	Row65	RAM73	
COM66	Row66	RAM66	Row74	RAM74	Row66	RAM74	Row66	RAM66	Row74	RAM74	Row66	RAM74	
COM67	Row67	RAM67	Row75	RAM75	Row67	RAM75	Row67	RAM67	Row75	RAM75	Row67	RAM75	
COM68	Row68	RAM68	Row76	RAM76	Row68	RAM76	Row68	RAM68	Row76	RAM76	Row68	RAM76	
COM69	Row69	RAM69	Row77	RAM77	Row69	RAM77	Row69	RAM69	Row77	RAM77	Row69	RAM77	
COM70	Row70	RAM70	Row78	RAM78	Row70	RAM78	Row70	RAM70	Row78	RAM78	Row70	RAM78	
COM71	Row71	RAM71	Row79	RAM79	Row71	RAM79	Row71	RAM71	Row79	RAM79	Row71	RAM79	
COM72	Row72	RAM72	Row80	RAM80	Row72	RAM80	Row72	RAM72	-	-	Row72	RAM80	
COM73	Row73	RAM73	Row81	RAM81	Row73	RAM81	Row73	RAM73	-	-	Row73	RAM81	
COM74	Row74	RAM74	Row82	RAM82	Row74	RAM82	Row74	RAM74	-	-	Row74	RAM82	
COM75	Row75	RAM75	Row83	RAM83	Row75	RAM83	Row75	RAM75	-	-	Row75	RAM83	
COM76	Row76	RAM76	Row84	RAM84	Row76	RAM84	Row76	RAM76	-	-	Row76	RAM84	
COM77	Row77	RAM77	Row85	RAM85	Row77	RAM85	Row77	RAM77	-	-	Row77	RAM85	
COM78	Row78	RAM78	Row86	RAM86	Row78	RAM86	Row78	RAM78	-	-	Row78	RAM86	
COM79	Row79	RAM79	Row87	RAM87	Row79	RAM87	Row79	RAM79	-	-	Row79	RAM87	
COM80	Row80	RAM80	Row88	RAM88	Row80	RAM88	-	-	-	-	-	-	
COM81	Row81	RAM81	Row89	RAM89	Row81	RAM89	-	-	-	-	-	-	
COM82	Row82	RAM82	Row90	RAM90	Row82	RAM90	-	-	-	-	-	-	
COM83	Row83	RAM83	Row91	RAM91	Row83	RAM91	-	-	-	-	-	-	
COM84	Row84	RAM84	Row92	RAM92	Row84	RAM92	-	-	-	-	-	-	
COM85	Row85	RAM85	Row93	RAM93	Row85	RAM93	-	-	-	-	-	-	
COM86	Row86	RAM86	Row94	RAM94	Row86	RAM94	-	-	-	-	-	-	
COM87	Row87	RAM87	Row95	RAM95	Row87	RAM95	-	-	-	-	-	-	
COM88	Row88	RAM88	Row0	RAM0	Row88	RAM0	-	-	Row0	RAM0	-	-	
COM89	Row89	RAM89	Row1	RAM1	Row89	RAM1	-	-	Row1	RAM1	-	-	
COM90	Row90	RAM90	Row2	RAM2	Row90	RAM2	-	-	Row2	RAM2	-	-	
COM91	Row91	RAM91	Row3	RAM3	Row91	RAM3	-	-	Row3	RAM3	-	-	
COM92	Row92	RAM92	Row4	RAM4	Row92	RAM4	-	-	Row4	RAM4	-	-	
COM93	Row93	RAM93	Row5	RAM5	Row93	RAM5	-	-	Row5	RAM5	-	-	
COM95	Row94	RAM94	Row6	RAM6	Row94	RAM6	-	-	Row6	RAM6	-	-	
COM95	Row95	RAM95	Row7	RAM7	Row95	RAM7	-	-	Row7	RAM7	-	-	
Display examples	(a)		(b)		(c)		(d)		(e)		(f)		



(a)

b)

c)

d)

(e)

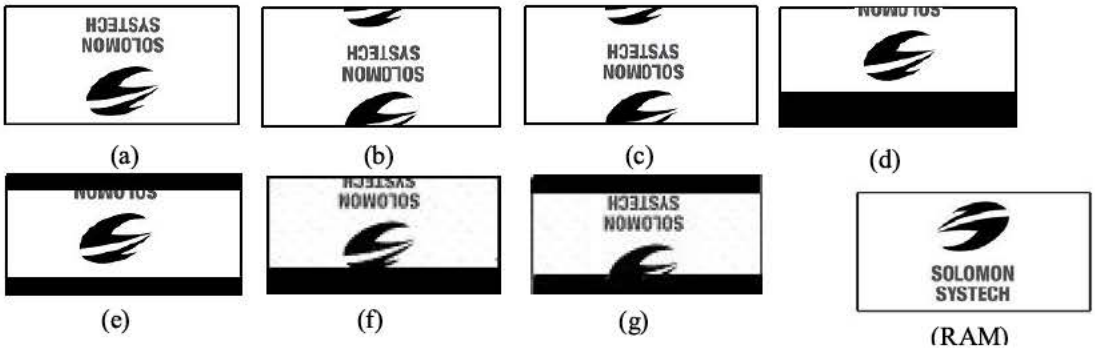
f)

(RAM)

Table 0-6: Example of Set Display Offset and Display Start Line with Remap

	Output																
	96		96		96		80		80		80		80				Set MUX ratio(A8h)
	Remap		Remap		R map		Remap		Remap		Remap		R map				COM Normal / Remapped (C0h / C8h)
Hardware pin	0		8		8		0		8		0		8				Display offset (D3h)
name	0		0		8		0		0		8		16				Display start line (A2h)
COM0	Row 95	RAM95	Row 7	RAM7	Row 95	RAM7	Row 79	RAM79	-	-	Row 79	RAM87	-	-			
COM1	Row 94	RAM94	Row 6	RAM6	Row 94	RAM6	Row 78	RAM78	-	-	Row 78	RAM86	-	-			
COM2	Row 93	RAM93	Row 5	RAM5	Row 93	RAM5	Row 77	RAM77	-	-	Row 77	RAM85	-	-			
COM3	Row 92	RAM92	Row 4	RAM4	Row 92	RAM4	Row 76	RAM76	-	-	Row 76	RAM84	-	-			
COM4	Row 91	RAM91	Row 3	RAM3	Row 91	RAM3	Row 75	RAM75	-	-	Row 75	RAM83	-	-			
COM5	Row 90	RAM90	Row 2	RAM2	Row 90	RAM2	Row 74	RAM74	-	-	Row 74	RAM82	-	-			
COM6	Row 89	RAM89	Row 1	RAM1	Row 89	RAM1	Row 73	RAM73	-	-	Row 73	RAM81	-	-			
COM7	Row 88	RAM88	Row 0	RAM0	Row 88	RAM0	Row 72	RAM72	-	-	Row 72	RAM80	-	-			
COM8	Row 87	RAM87	Row 95	RAM95	Row 87	RAM95	Row 71	RAM71	Row 79	RAM79	Row 71	RAM79	Row 79	RAM95			
COM9	Row 86	RAM86	Row 94	RAM94	Row 86	RAM94	Row 70	RAM70	Row 78	RAM78	Row 70	RAM78	Row 78	RAM94			
COM10	Row 85	RAM85	Row 93	RAM93	Row 85	RAM93	Row 69	RAM69	Row 77	RAM77	Row 69	RAM77	Row 77	RAM93			
COM11	Row 84	RAM84	Row 92	RAM92	Row 84	RAM92	Row 68	RAM68	Row 76	RAM76	Row 68	RAM76	Row 76	RAM92			
COM12	Row 83	RAM83	Row 91	RAM91	Row 83	RAM91	Row 67	RAM67	Row 75	RAM75	Row 67	RAM75	Row 75	RAM91			
COM13	Row 82	RAM82	Row 90	RAM90	Row 82	RAM90	Row 66	RAM66	Row 74	RAM74	Row 66	RAM74	Row 74	RAM90			
COM14	Row 81	RAM81	Row 89	RAM89	Row 81	RAM89	Row 65	RAM65	Row 73	RAM73	Row 65	RAM73	Row 73	RAM89			
COM15	Row 80	RAM80	Row 88	RAM88	Row 80	RAM88	Row 64	RAM64	Row 72	RAM72	Row 64	RAM72	Row 72	RAM88			
COM16	Row 79	RAM79	Row 87	RAM87	Row 79	RAM87	Row 63	RAM63	Row 71	RAM71	Row 63	RAM71	Row 71	RAM87			
COM17	Row 78	RAM78	Row 86	RAM86	Row 78	RAM86	Row 62	RAM62	Row 70	RAM70	Row 62	RAM70	Row 70	RAM86			
COM18	Row 77	RAM77	Row 85	RAM85	Row 77	RAM85	Row 61	RAM61	Row 69	RAM69	Row 61	RAM69	Row 69	RAM85			
COM19	Row 76	RAM76	Row 84	RAM84	Row 76	RAM84	Row 60	RAM60	Row 68	RAM68	Row 60	RAM68	Row 68	RAM84			
COM20	Row 75	RAM75	Row 83	RAM83	Row 75	RAM83	Row 59	RAM59	Row 67	RAM67	Row 59	RAM67	Row 67	RAM83			
COM21	Row 74	RAM74	Row 82	RAM82	Row 74	RAM82	Row 58	RAM58	Row 66	RAM66	Row 58	RAM66	Row 66	RAM82			
COM22	Row 73	RAM73	Row 81	RAM81	Row 73	RAM81	Row 57	RAM57	Row 65	RAM65	Row 57	RAM65	Row 65	RAM81			
COM23	Row 72	RAM72	Row 80	RAM80	Row 72	RAM80	Row 56	RAM56	Row 64	RAM64	Row 56	RAM64	Row 64	RAM80			
COM24	Row 71	RAM71	Row 79	RAM79	Row 71	RAM79	Row 55	RAM55	Row 63	RAM63	Row 55	RAM63	Row 63	RAM79			
COM25	Row 70	RAM70	Row 78	RAM78	Row 70	RAM78	Row 54	RAM54	Row 62	RAM62	Row 54	RAM62	Row 62	RAM78			
COM26	Row 69	RAM69	Row 77	RAM77	Row 69	RAM77	Row 53	RAM53	Row 61	RAM61	Row 53	RAM61	Row 61	RAM77			
COM27	Row 68	RAM68	Row 76	RAM76	Row 68	RAM76	Row 52	RAM52	Row 60	RAM60	Row 52	RAM60	Row 60	RAM76			
COM28	Row 67	RAM67	Row 75	RAM75	Row 67	RAM75	Row 51	RAM51	Row 59	RAM59	Row 51	RAM59	Row 59	RAM75			
COM29	Row 66	RAM66	Row 74	RAM74	Row 66	RAM74	Row 50	RAM50	Row 58	RAM58	Row 50	RAM58	Row 58	RAM74			
COM30	Row 65	RAM65	Row 73	RAM73	Row 65	RAM73	Row 49	RAM49	Row 57	RAM57	Row 49	RAM57	Row 57	RAM73			
COM31	Row 64	RAM64	Row 72	RAM72	Row 64	RAM72	Row 48	RAM48	Row 56	RAM56	Row 48	RAM56	Row 56	RAM72			
COM32	Row 63	RAM63	Row 71	RAM71	Row 63	RAM71	Row 47	RAM47	Row 55	RAM55	Row 47	RAM55	Row 55	RAM71			
COM33	Row 62	RAM62	Row 70	RAM70	Row 62	RAM70	Row 46	RAM46	Row 54	RAM54	Row 46	RAM54	Row 54	RAM70			
COM34	Row 61	RAM61	Row 69	RAM69	Row 61	RAM69	Row 45	RAM45	Row 53	RAM53	Row 45	RAM53	Row 53	RAM69			
COM35	Row 60	RAM60	Row 68	RAM68	Row 60	RAM68	Row 44	RAM44	Row 52	RAM52	Row 44	RAM52	Row 52	RAM68			
COM36	Row 59	RAM59	Row 67	RAM67	Row 59	RAM67	Row 43	RAM43	Row 51	RAM51	Row 43	RAM51	Row 51	RAM67			
COM37	Row 58	RAM58	Row 66	RAM66	Row 58	RAM66	Row 42	RAM42	Row 50	RAM50	Row 42	RAM50	Row 50	RAM66			
COM38	Row 57	RAM57	Row 65	RAM65	Row 57	RAM65	Row 41	RAM41	Row 49	RAM49	Row 41	RAM49	Row 49	RAM65			
COM39	Row 56	RAM56	Row 64	RAM64	Row 56	RAM64	Row 40	RAM40	Row 48	RAM48	Row 40	RAM48	Row 48	RAM64			
COM40	Row 55	RAM55	Row 63	RAM63	Row 55	RAM63	Row 39	RAM39	Row 47	RAM47	Row 39	RAM47	Row 47	RAM63			
COM41	Row 54	RAM54	Row 62	RAM62	Row 54	RAM62	Row 38	RAM38	Row 46	RAM46	Row 38	RAM46	Row 46	RAM62			
COM42	Row 53	RAM53	Row 61	RAM61	Row 53	RAM61	Row 37	RAM37	Row 45	RAM45	Row 37	RAM45	Row 45	RAM61			
COM43	Row 52	RAM52	Row 60	RAM60	Row 52	RAM60	Row 36	RAM36	Row 44	RAM44	Row 36	RAM44	Row 44	RAM60			
COM44	Row 51	RAM51	Row 59	RAM59	Row 51	RAM59	Row 35	RAM35	Row 43	RAM43	Row 35	RAM43	Row 43	RAM59			
COM45	Row 50	RAM50	Row 58	RAM58	Row 50	RAM58	Row 34	RAM34	Row 42	RAM42	Row 34	RAM42	Row 42	RAM58			
COM46	Row 49	RAM49	Row 57	RAM57	Row 49	RAM57	Row 33	RAM33	Row 41	RAM41	Row 33	RAM41	Row 41	RAM57			
COM47	Row 48	RAM48	Row 56	RAM56	Row 48	RAM56	Row 32	RAM32	Row 40	RAM40	Row 32	RAM40	Row 40	RAM56			
COM48	Row 47	RAM47	Row 55	RAM55	Row 47	RAM55	Row 31	RAM31	Row 39	RAM39	Row 31	RAM39	Row 39	RAM55			
COM49	Row 46	RAM46	Row 54	RAM54	Row 46	RAM54	Row 30	RAM30	Row 38	RAM38	Row 30	RAM38	Row 38	RAM54			
COM50	Row 45	RAM45	Row 53	RAM53	Row 45	RAM53	Row 29	RAM29	Row 37	RAM37	Row 29	RAM37	Row 37	RAM53			
COM51	Row 44	RAM44	Row 52	RAM52	Row 44	RAM52	Row 28	RAM28	Row 36	RAM36	Row 28	RAM36	Row 36	RAM52			
COM52	Row 43	RAM43	Row 51	RAM51	Row 43	RAM51	Row 27	RAM27	Row 35	RAM35	Row 27	RAM35	Row 35	RAM51			
COM53	Row 42	RAM42	Row 50	RAM50	Row 42	RAM50	Row 26	RAM26	Row 34	RAM34	Row 26	RAM34	Row 34	RAM50			
COM54	Row 41	RAM41	Row 49	RAM49	Row 41	RAM49	Row 25	RAM25	Row 33	RAM33	Row 25	RAM33	Row 33	RAM49			
COM55	Row 40	RAM40	Row 48	RAM48	Row 40	RAM48	Row 24	RAM24	Row 32	RAM32	Row 24	RAM32	Row 32	RAM48			
COM56	Row 39	RAM39	Row 47	RAM47	Row 39	RAM47	Row 23	RAM23	Row 31	RAM31	Row 23	RAM31	Row 31	RAM47			
COM57	Row 38	RAM38	Row 46	RAM46	Row 38	RAM46	Row 22	RAM22	Row 30	RAM30	Row 22	RAM30	Row 30	RAM46			
COM58	Row 37	RAM37	Row 45	RAM45	Row 37	RAM45	Row 21	RAM21	Row 29	RAM29	Row 21	RAM29	Row 29	RAM45			
COM59	Row 36	RAM36	Row 44	RAM44	Row 36	RAM44	Row 20	RAM20	Row 28	RAM28	Row 20	RAM28	Row 28	RAM44			
COM60	Row 35	RAM35	Row 43	RAM43	Row 35	RAM43	Row 19	RAM19	Row 27	RAM27	Row 19	RAM27	Row 27	RAM43			
COM61	Row 34	RAM34	Row 42	RAM42	Row 34	RAM42	Row 18	RAM18	Row 26	RAM26	Row 18	RAM26	Row 26	RAM42			
COM62	Row 33	RAM33	Row 41	RAM41	Row 33	RAM41	Row 17	RAM17	Row 25	RAM25	Row 17	RAM25	Row 25	RAM41			
COM63	Row 32	RAM32	Row 40	RAM40	Row 32	RAM40	Row 16	RAM16	Row 24	RAM24	Row 16	RAM24	Row 24	RAM40			
COM64	Row 31	RAM31	Row 39	RAM39	Row 31	RAM39	Row 15	RAM15	Row 23	RAM23	Row 15	RAM23	Row 23	RAM39			
COM65	Row 30	RAM30	Row 38	RAM38	Row 30	RAM38	Row 14	RAM14	Row 22	RAM22	Row 14	RAM22	Row 22	RAM38			
COM66	Row 29	RAM29	Row 37	RAM37	Row 29	RAM37	Row 13	RAM13	Row 21	RAM21	Row 13	RAM21	Row 21	RAM37			
COM67	Row 28	RAM28	Row 36	RAM36	Row 28	RAM36	Row 12	RAM12	Row 20	RAM20	Row 12	RAM20	Row 20	RAM36			
COM68	Row 27	RAM27	Row 35	RAM35	Row 27	RAM35	Row 11	RAM11	Row 19	RAM19	Row 11	RAM19	Row 19	RAM35			
COM69	Row 26	RAM26	Row 34	RAM34	Row 26	RAM34	Row 10	RAM10	Row 18	RAM18	Row 10	RAM18	Row 18	RAM34			
COM70	Row 25	RAM25	Row 33	RAM33	Row 25	RAM33	Row 9	RAM9	Row 17	RAM17	Row 9	RAM17	Row 17	RAM33			
COM71	Row 24	RAM24	Row 32	RAM32	Row 24	RAM32	Row 8	RAM8	Row 16	RAM16	Row 8	RAM16	Row 16	RAM32			
COM72	Row 23	RAM23	Row 31	RAM31	Row 23	RAM31	Row 7	RAM7	Row 15	RAM15	Row 7	RAM15	Row 15	RAM31			

	Output														
	96		96		96		80		80		80		80		Set MUX ratio(A8h)
	Remap		Remap		Remap		Remap		Remap		Remap		Remap		COM Normal / Remapped (C0h / C8h)
Hardware	0		8		0		0		8		0		8		Display offset (D3h)
pin name	0		0		8		0		0		8		16		Display start line (A2h)
COM73	Row 22	RAM22	Row 30	RAM30	Row 22	RAM30	Row 6	RAM6	Row 14	RAM14	Row 6	RAM14	Row 14	RAM30	
COM74	Row 21	RAM21	Row 29	RAM29	Row 21	RAM29	Row 5	RAM5	Row 13	RAM13	Row 5	RAM13	Row 13	RAM29	
COM75	Row 20	RAM20	Row 28	RAM28	Row 20	RAM28	Row 4	RAM4	Row 12	RAM12	Row 4	RAM12	Row 12	RAM28	
COM76	Row 19	RAM19	Row 27	RAM27	Row 19	RAM27	Row 3	RAM3	Row 11	RAM11	Row 3	RAM11	Row 11	RAM27	
COM77	Row 18	RAM18	Row 26	RAM26	Row 18	RAM26	Row 2	RAM2	Row 10	RAM10	Row 2	RAM10	Row 10	RAM26	
COM78	Row 17	RAM17	Row 25	RAM25	Row 17	RAM25	Row 1	RAM1	Row 9	RAM9	Row 1	RAM9	Row 9	RAM25	
COM79	Row 16	RAM16	Row 24	RAM24	Row 16	RAM24	Row 0	RAM0	Row 8	RAM8	Row 0	RAM8	Row 8	RAM24	
COM80	Row 15	RAM15	Row 23	RAM23	Row 15	RAM23	-	-	Row 7	RAM7	-	-	Row 7	RAM23	
COM81	Row 14	RAM14	Row 22	RAM22	Row 14	RAM22	-	-	Row 6	RAM6	-	-	Row 6	RAM22	
COM82	Row 13	RAM13	Row 21	RAM21	Row 13	RAM21	-	-	Row 5	RAM5	-	-	Row 5	RAM21	
COM83	Row 12	RAM12	Row 20	RAM20	Row 12	RAM20	-	-	Row 4	RAM4	-	-	Row 4	RAM20	
COM84	Row 11	RAM11	Row 19	RAM19	Row 11	RAM19	-	-	Row 3	RAM3	-	-	Row 3	RAM19	
COM85	Row 10	RAM10	Row 18	RAM18	Row 10	RAM18	-	-	Row 2	RAM2	-	-	Row 2	RAM18	
COM86	Row 9	RAM9	Row 17	RAM17	Row 9	RAM17	-	-	Row 1	RAM1	-	-	Row 1	RAM17	
COM87	Row 8	RAM8	Row 16	RAM16	Row 8	RAM16	-	-	Row 0	RAM0	-	-	Row 0	RAM16	
COM88	Row 7	RAM7	Row 15	RAM15	Row 7	RAM15	-	-	-	-	-	-	-	-	
COM89	Row 6	RAM6	Row 14	RAM14	Row 6	RAM14	-	-	-	-	-	-	-	-	
COM90	Row 5	RAM5	Row 13	RAM13	Row 5	RAM13	-	-	-	-	-	-	-	-	
COM91	Row 4	RAM4	Row 12	RAM12	Row 4	RAM12	-	-	-	-	-	-	-	-	
COM92	Row 3	RAM3	Row 11	RAM11	Row 3	RAM11	-	-	-	-	-	-	-	-	
COM93	Row 2	RAM2	Row 10	RAM10	Row 2	RAM10	-	-	-	-	-	-	-	-	
COM94	Row 1	RAM1	Row 9	RAM9	Row 1	RAM9	-	-	-	-	-	-	-	-	
COM95	Row 0	RAM0	Row 8	RAM8	Row 0	RAM8	-	-	-	-	-	-	-	-	
Display examples	(a)		(b)		(c)		(d)		(e)		(f)		(g)		



xviii. Set Display Clock Divide Ratio/ Oscillator Frequency (D5h)

This command consists of two functions:

- Display Clock Divide Ratio (D) (A[3:0])
  Set the divide ratio to generate DCLK (Display Clock) from CLK. The divide ratio is from 1 to 16, with reset value = 0000b. Please refer to section 6.3 for the details relationship of DCLK and CLK.

- Oscillator Frequency (A[7:4])
  Program the oscillator frequency Fosc that is the source of CLK if CLS pin is pulled high. The 4-bit value results in 16 different frequency settings available. The default setting is 1011b.

xix. Set Pre-charge Period (D9h)

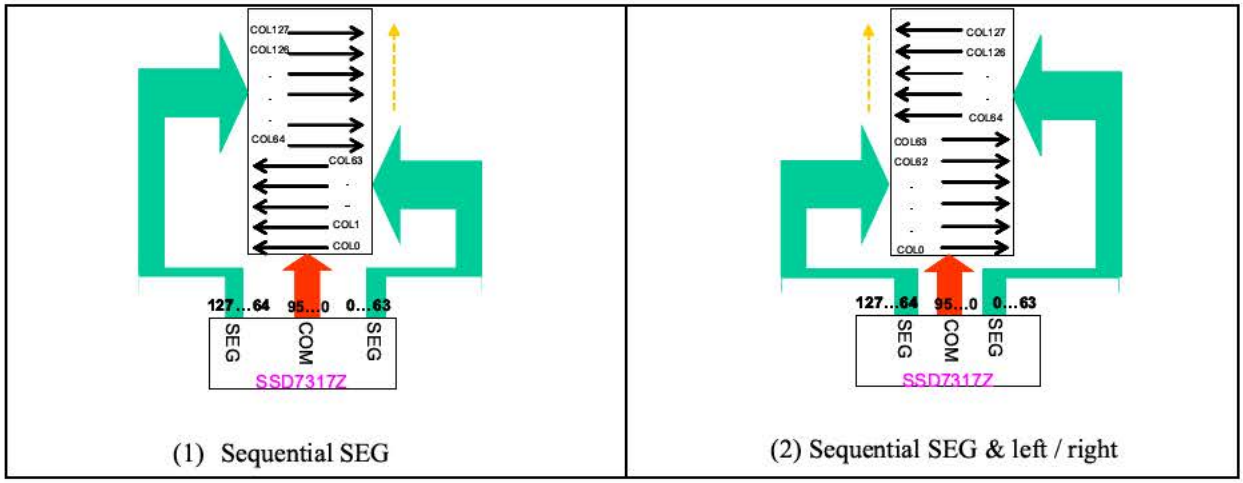
This command is used to set the duration of the pre-charge period. The interval is counted in number of DCLK, where RESET equals to 4 DCLKs.

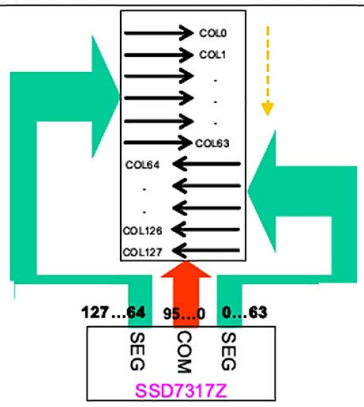
xx. Set SEG Pins Hardware Configuration (DAh)

This command sets the SEG signals pin configuration to match the OLED panel hardware layout. SEG Odd / Even (Left / Right) and Top / Bottom connections are software selectable, thus there are total of 8 cases and they are shown on the followings:

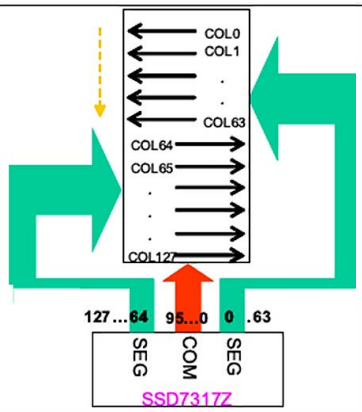
Table 0-7 : SEG Pins Hardware Configuration

Case no.	Oddeven (1) / Sequential (0) Command : DAh -> A[4]	SEG Remap Command : A0h / A1h	Left / Right Swap Command : DAh -> A[5]	Remark
1	0	0	0	
2	0	0	1	
3	0	1	0	
4	0	1	1	
5	1	0	0	Default
6	1	0	1	
7	1	1	0	
8	1	1	1	

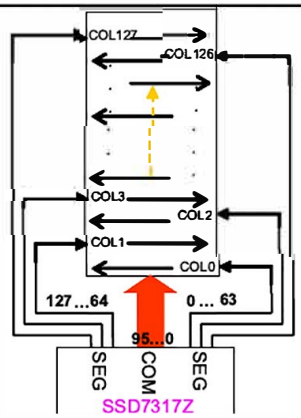




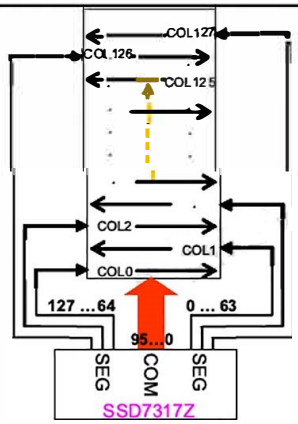
(3) Sequential SEG & SEG remap



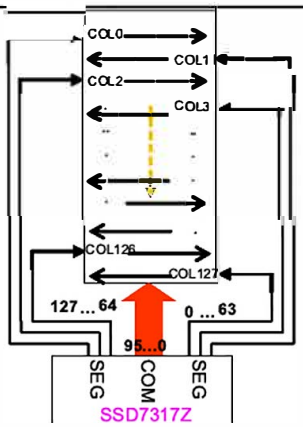
(4) Sequential SEG & SEG remap & left / right



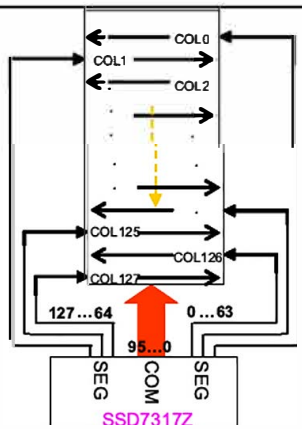
(5) Odd / even SEG



(6) Odd / even SEG & left / right



(7) Odd / even SEG & SEG remap



(8) Odd / even SEG & SEG remap & left / right

Note:

(1) The above eight figures are all with bump pads being faced up.

xxi. Set V_{COMH} Deselect Level (DBh)

This command adjusts the VCOMH regulator output. Please refer Table 0-2 for details.

xxii. NOP (E3h)

No Operation Command.

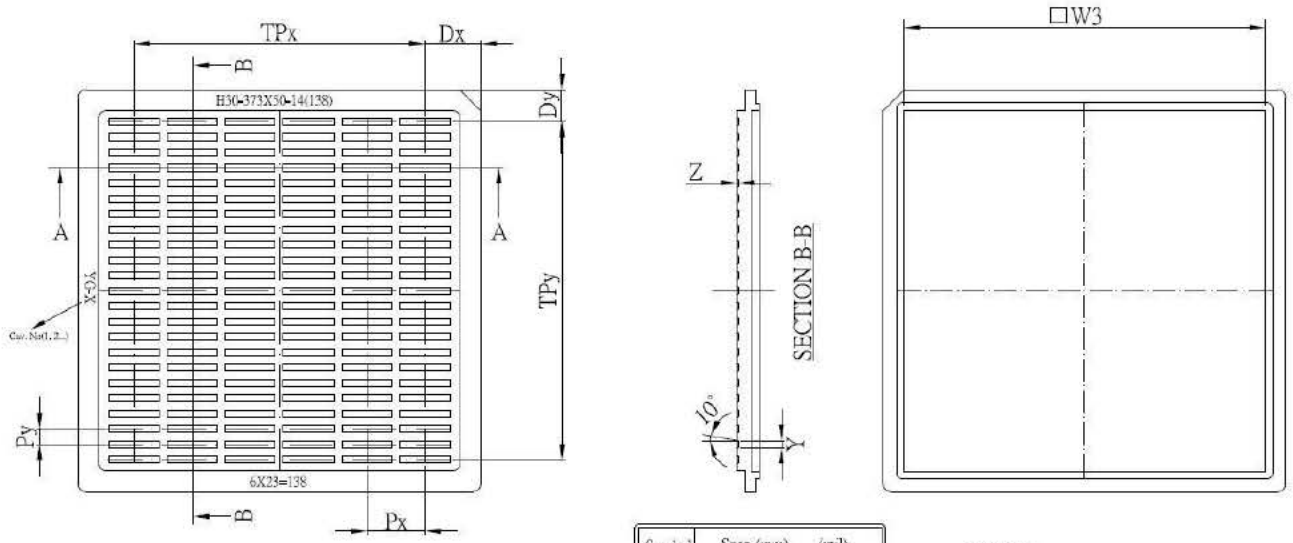
xxiii. Set Command Lock (FDh)

This double byte command is used to lock the OLED driver IC from accepting any command except itself. After entering FDh 16h (A[2]=1b), the OLED driver IC will not respond to any newly-entered command (except FDh 12h A[2]=0b) and there will be no memory access. This is called “Lock” state. That means the OLED driver IC ignore all the commands (except FDh 12h A[2]=0b) during the “Lock” state.

Entering FDh 12h (A[2]=0b) can unlock the OLED driver IC. That means the driver IC resumes from the “Lock” state, and the driver IC will then respond to the command and memory access.

Appendix IV: SSD7317Z Die Tray Information

Figure 1-11: – SSD7317Z Die Tray drawing



Symbol	Spec (mm)	(mil)
W1	76.00±0.10	(2992)
W2	68.00±0.10	(2677)
W3	68.30±0.10	(2689)
Dx	10.50±0.10	(413)
TPx	55.00±0.10	(2165)
Dy	6.10±0.10	(240)
TPy	63.80±0.10	(2512)
Px	11.00±0.05	(433)
Py	2.90±0.05	(114)
X	9.47±0.05	(373)
Y	1.27±0.05	(50)
Z	0.35±0.05	(14)
N	138(pocket number)	

Remark:
1. Depth of text : Max. 0.1mm
2. Tray material : ABS
3. Tray Color Code: Black
4. Surface Resistance: 10^{9}~10^{12}Ω/SQ
5. Tray Warpage: Max. ±0.1mm
6. Pocket Bottom: Rough Surface